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THERMAL STRESS MITIGATION OF SINGLE-PHASE SINEWAVE INVERTER BY USING DOUBLE SWITCH H BRIDGE CONFIGURATION

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Mohammad Mousa Ahmad Hushki

This thesis is submitted in partial fulfilment of the requirements for the degree of Master of Science in Electrical Engineering

Under the supervision of Professor Hussain Shareef

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Declaration of Original Work

I, Mohammad Mousa Ahmad Hushki, the undersigned, a graduate student at the United Arab Emirates University (UAEU), and the author of this thesis entitled "*Thermal Stress Mitigation of Single-Phase Sinewave Inverter by Using Double Switch H Bridge Configuration*", hereby, solemnly declare that this is the original research work done by me under the supervision of Prof. Hussain Shareef, in the College of Engineering at UAEU. This work has not previously formed the basis for the award of any academic degree, diploma or a similar title at this or any other university. Any materials borrowed from other sources (whether published or unpublished) and relied upon or included in my thesis have been properly cited and acknowledged in accordance with appropriate academic conventions. I further declare that there is no potential conflict of interest with respect to the research, data collection, authorship, presentation and/or publication of this thesis.

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   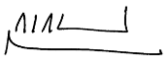

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Abstract

The increasing demand for renewable energies and the ongoing advancement in the industry require continuously evolving power converters in terms of efficiency, power density, and reliability. Furthermore, power converters' applications in harsh and remote environments such as offshore wind turbines demand robust and reliable designs to help reduce operational costs. Power switch failure is a critical reliability issue that leads to the converter going out of service, causing an unscheduled maintenance event. The main reason behind power switch failure is thermal cycling. Therefore, the first part of this thesis attempts to develop an effective double switch H bridge inverter topology aiming to lessen thermal cycling subjected to power switches, increasing the expected lifetime of power switches and improving the system's overall reliability, and reduces the operational costs.

Meanwhile, the second focus of the thesis is to develop a visual interpretation of an empirical lifetime estimation model that enables the evaluation of the proposed inverter topology compared to the conventional topology. This is done by producing a novel lifetime improvement evaluation curve based on a common empirical lifetime estimation model using MATLAB®. Moreover, the interpretation of the empirical lifetime estimation models as lifetime improvement evaluation curve helps to bridge the gap between any thermal condition change and its impact on the expected lifetime. The percentage reduction in the junction's median temperature $\%T_{jm\_red}$, and the percentage reduction in the temperature swing $\%\Delta T_{j\_red}$ are taken as the main contributors to the change in the switch's estimated cycles to failure N_f. The effectiveness of the proposed topology was verified via simulation of the thermal parameters for the two topologies via PLECS® software. Several test scenarios were performed to illustrate the impact of shifting from the conventional topology to the proposed topology. Following that, numerous loading conditions were considered to perform an extensive comparative analysis between the proposed and the conventional topologies. Three power factor values were adopted at high, medium, and low values; to compare the two topologies while covering an adequate loading range for each power factor value. The assessment indices, namely, Life Prolonging Factor (LPF), and the average LPF (in a temperature range) obtained promising results, especially

for high loading levels conditions. The LPF reached values more than ‘2’ under some conditions, indicating a lifetime increase of more than double. Furthermore, the average LPF in a specific temperature range indicated promising results in general for common loading conditions with an advantage for higher loading conditions over lower loading conditions.

Keywords: Power Conversion, Inverters, Thermal Cycling, Semiconductors Lifetime Estimation, Reliability.

Title and Abstract (in Arabic)

تخفيف العبء الحراري على عواكس الجهد احادية الطور

الملخص

ان الطلب المتزايد على انظمة الطاقة المتجددة والتطورات الصناعية الجارية تتطلب تطوير مستمر لاجهزة الكترونيات القدرة المستخدمة في تحويل الطاقة من شكل لآخر (محولات القدرة) من حيث الكفاءة، والقدرة لكل وحدة حجم والموثوقية. اضافة الى ذلك، تطبيقات محولات القدرة الواقعة تحت ظروف صعبة وفي مناطق نائية مثل مولدات طاقة الرياح المنصوبة في جزر اصطناعية بحرية تتطلب تصاميم ذات موثوقية عالية نظرا لتكاليف الصيانة المرتفعة في حالة الاعطال. ان اعطال مفاتيح اشباه الموصلات تعتبر من اهم مشاكل موثوقية محولات القدرة بحيث انها تؤدي عادة الى توقف الوحدة تماما عن العمل وانقطاع تزويد الاحمال بالطاقة اللازمة، مما يترتب عليه متطلبات صيانة غير مجدولة لدى الجهة المشغلة. المحرك الاساسي وراء اعطال اشباه الموصلات بالتطبيقات ذات القدرة العالية هي ظاهرة التدوير الحراري. لذا، فالهدف الاول من هذه الرسالة يتمثل بتطوير دائرة فعالة لجهاز عاكس الجهد احادي الطور تهدف لتخفيف ظاهرة العبئ الحراري الذي تتعرض له اشباه الموصلات في الجهاز مما يحسن من العمر المتوقع لاشباه الموصلات، وبالتالي يرفع من مستوى موثوقية النظام ككل ويقلل من مصاريف التشغيل والصيانة.

الهدف الثاني لهذه الرسالة يتمثل في تطوير تمثيل مرئي لمعادلات تقدير اعمار اشباه الموصلات المعتمدة على البيانات التجريبية في مجال اشباه الموصلات، مما يساعد في تقييم النظام المقترح في هذه الرسالة ومقارنته مع نظام التشغيل التقليدي لاجهزة عواكس الجهد احادية الطور. يتم تقييم اداء الدائرة المقترحة عن طريق تطوير منحنى تقييم تحسين العمر الافتراضي لاشباه الموصلات باستخدام برمجية MATLAB®. علاوة على ذلك، تمثيل انظمة تقدير اعمار اشباه الموصلات على شكل (منحنى تقييم درجة تحسين العمر الافتراضي لاشباه الموصلات) يساعد في فهم الاثر المباشر لأي تغيير يطرأ على الظرف الحراري لاشباه الموصلات على العمر الافتراضي المتوقع لها. تم اعتماد نسبة الانخفاض المئوية على درجة الحرارة المتوسطة لشبه الموصل $\%T_{jm\_red}$ ونسبة الانخفاض المئوية على درجة تأرجح حرارة شبه الموصل $\%\Delta T_{j\_red}$ كعاملين اساسيين لتقدير عدد مرات التدوير الحراري المؤدية لفشل شبه الموصل N_f. تم التحقق من فعالية الدائرة

المقترحة عن طريق محاكاة الظرف الحراري لاشباه الموصلات ومقارنة الدائرة المقترحة مع الدائرة التقليدية باستخدام برمجية PLECS®. تم اجراء اختبارات لعدة ظروف تشغيلية بهدف توضيح اثر تبني الدائرة المقترحة بدلا من الدائرة التقليدية على العمر التقديري لاشباه الموصلات وبالتالي الوصول لانظمة ذات موثوقية اعلى. يتبع ذلك دراسة نتائج النظامين المقترح والتقليدي ومقارنتهما في عدد من ظروف التحميل المختلفة. بحيث تم اعتماد ثلاث قيم لمعامل القدرة حتى يتسنى مقارنة النظامين تحت ظروف التحميل المختلفة المتمثلة في معامل القدرة ودرجة التحميل عند معامل القدرة. مؤشرات تقييم الاداء المتمثلة في معامل زيادة العمر LPF ومتوسط معامل زيادة العمر (لكل فئة حرارية محددة) قدمت نتائج مبشرة خصوصا في ظروف التحميل العالية. معامل زيادة العمر تعدى "2" في بعض الحالات مما يشير الى زيادة العمر الافتراضي لاشباه الموصلات لأكثر من ضعف العمر الاصلي لنفس الظرف التشغيلي في حالة الدائرة التقليدية. زيادة على ذلك، مؤشر متوسط زيادة العمر (لكل فئة حرارية محددة) يشير الى نتائج مبشرة للدائرة والنظام المقترح خصوصا في ظروف التحميل العالية بالمقارنة مع ظروف التحميل المنخفضة.

مفاهيم البحث الرئيسية: تحويل الطاقة، عاكسات الجهود، التدوير الحراري، تقدير اعمار اشباه الموصلات، الموثوقية.

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Dedication

To my beloved parents and family…….
To my dear friends who always motivated me …….

Table of Contents

List of Tables

List of Figures

List of Abbreviations

CMV	Common Mode Voltage
CPWM	Continuous Pulse Width Modulation
CTE	Coefficient of Thermal Expansion
DCTM	Dynamic Compact Thermal Model
DPWM	Discontinuous Pulse Width Modulation
FEA	Finite Element Analysis
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
ISI	Impedance Source Inverter
LPF	Life-Prolonging Factor
MBC	Maximum-Boost Modulation
MBMSV	Maximum-Boost Modified Space Vector
MBSV	Maximum-Boost Space Vector
MCB	Maximum-Constant-Boost
MMC	Modular Multi-level Converter
PF	Power Factor
PMSM	Permanent Magnet Synchronous Motor
PoF	Physics of Failure
PV	Photovoltaic
PWM	Pulse Width Modulation
SBMSV	Simple-Boost Modified Space Vector
SPWM	Sinusoidal Pulse Width Modulation

SVPWM	Space Vector Pulse Width Modulation
TDDB	Time-Dependent Dielectric Breakdown
THD	Total Harmonic Distortion
THIPWM	Third Harmonic Injection Pulse Width Modulation
TSEP	Temperature Sensitive Electrical Parameter
TTIC	Transient Thermal Impedance Curve
UPWM	Unipolar Pulse Width Modulation
VFDs	Variable Frequency Drives
VSI	Voltage Source Inverter

List of Symbols

N_f	Cycles to Failure
T_{jm}	Median Junction Temperature
ΔT_j	Junction Temperature Swing
f_c	Cycling Frequency
$\%\Delta T_{j\_red}$	Percentage Reduction in Junction Temperature Swing
$\%T_{jm\_red}$	Percentage Reduction in Median Junction Temperature
T_j	Junction Temperature
τ	Time Constant
Z_{j-a}	Junction to Ambient Thermal Impedance
P_{cond}	Conduction Power Losses
P_{sw}	Switching Power Losses
R_{on}	On Resistance
I_{RMS}	RMS Current
V_{DS}	MOSFET's Drain-Source Voltage
I_D	MOSFET's Drain Current
V_{CE}	IGBT's Collector-Emitter Voltage
I_C	IGBT's Collector Current
T_{on}	Duration of the Switch's Turning On event
T_{off}	Duration of the Switch's Turning Off event
V_s	Permanent Magnet Synchronous Motor's Stator Voltage
m	Modulation Index
Ea	Activation Energy

K_b	Boltzmann Constant
V_o	Output Voltage
V_{leg}	Inverter's Node Voltage
f_f	Fundamental Frequency
T_s	Switching Signal's time period
C_n	Fundamental cycle's number
T_t	Temperature at time (t)
T_i	Initial Temperature
$Lifetime_{(p)}$	Proposed method's power switch lifetime (in years)
$Lifetime_{(c)}$	Conventional method's power switch lifetime (in years)
T_{jm_conv}	Median Junction Temperature in case of the conventional topology
T_{jm_prop}	Median Junction Temperature in case of the proposed topology

Chapter 1: Introduction

1.1 Research Background

Power converters reserved their seat in the first row of various applications, from High Voltage DC (HVDC) lines to industrial motor drives, down to small laptop chargers. Such converters can be found following the same logic and principle of operation oriented around switching, with proper considerations to suit the purpose and the amount of power to be passed through it. The three key concerns are mainly considered when a power converter is designed: power density, efficiency, and reliability.

Recently, power converters are gaining more demand in quantity and quality in numerous applications. Moreover, reliability is of great importance among the converters' design key concerns since the converters operating in remote areas such as offshore wind turbines suffer from high operational and maintenance costs. Hence, an unscheduled failure event caused by the inverter would be a headache for the operator as well as the customer if the failure led to a power outage. Therefore, designs and topologies that are oriented towards reliability are needed.

One of the major causes of electronic components to fail is thermal cycling. The converters' power switches endure thermal cycling throughout their operation until the thermal cycling or a catastrophic event cause failure of the switch. Thermal cycling is directly affected by the nature of power losses that the switch endures. Generally, switches suffer from two major losses: switching and conduction losses. As their names imply, switching losses occur when switching on/off, and conduction losses are present whenever the switch is conducting current. The total power loss amplitude and instance of occurrence determine the thermal cycling intensity that the switch goes

through. Generally, mitigating the thermal cycling subjected to power switches has two main types. The first type is to control the losses on the power switch, either by reducing the losses at specific instances or introducing extra losses at other instances. The second type is to control the cooling system to reduce the thermal cycling effect.

1.2 Problem Statement

Although power switches' thermal cycling is unavoidable, its mitigation is of great importance due to its negative impact on reliability. With every rise and drop of the internal components' temperature, slight damage occurs between the different materials comprising the semiconductor switch. A famous index of components' reliability is the cycles to failure (N_f), which relies mainly on the junction's median temperature (T_{jm}), and the temperature swing (ΔT_j). Consequently, reducing (T_{jm}) or (ΔT_j) will lead to higher N_f, and reducing the cycling frequency (f_c) will lead to a better lifetime in years for the same N_f. Therefore, this study attempts to develop a simple and effective topology for single-phase inverters that mitigates the overall thermal cycling on the inverter's power switches, hence, achieve a better lifetime in years per switch.

Moreover, N_f is commonly determined by using lifetime estimation models which usually relies on the variables T_{jm}, and ΔT_j. Although, the form of lifetime estimation models does not clearly show the effect of improving T_{jm} or ΔT_j on N_f. Therefore, this study also attempts to develop a better interpretation of a famous empirical lifetime estimation model in a way that directly shows the impact of mitigating T_{jm}, and ΔT_j on N_f using a novel lifetime improvement evaluation curve.

Several techniques have been developed to mitigate thermal cycling. However, these techniques were oriented toward thermal cycling that occurs over minutes or hours. Thus, this creates a gap for the thermal cycling at the fundamental frequency of the output current. The output current's fundamental frequency is famously known to be 50 Hz or 60 Hz in the case of power inverters connected to the grid or supplying domestic loads, while the frequency can even go beyond that for the case of Variable Frequency Drives (VFDs) to several hundreds of Hertz.

For instance, [1]–[4] used active cooling control to mitigate thermal cycling and improve reliability. However, the targeted thermal cycling was in the low frequency end. Therefore, their results are given with a time division of 500s, indicating that the improved thermal cycling due to their work is in the very low frequency side where the temperature is cycling once every several minutes.

Considering the development of renewable energy resources over the years, power converters demand higher reliability since they are responsible for conditioning the clean energy to become usable in the most efficient and compact manner possible. Hence, designs oriented toward improving the thermal cycling at the inverters' output fundamental frequency are needed.

1.3 Objectives of the Research

The objectives of the research are as follows:

I. To develop a single-phase inverter topology that can effectively improve reliability by mitigating the thermal cycling on power switches.

II. To propose a better interpretation of a famous empirical lifetime estimation model, which helps bridge the effect of thermal conditions change with their impact on the estimated lifetime.

III. To validate the proposed topology's performance and compare it with the conventional topology under adequate loading conditions.

1.4 The Scope of the Research

The initial work conducted in this research focuses on developing a single-phase inverter bridge. Currently, no previous research has served the thermal cycling with the order of the fundamental frequency of the inverter's output. This research aims to show the effect of any change in the thermal parameters (T_{jm}, ΔT_j, f_c) on the expected lifetime, so this work may also benefit any following research work aiming to target these parameters in hopes of reliability improvement.

For validation purposes, the proposed topology is simulated with various loading conditions on MATLAB®, while the thermal aspect of the circuit is simulated using PLECS®. Moreover, the performance evaluation considered to assess the effectiveness and impact of the proposed topology is based on a famous empirical lifetime estimation model. Moreover, the contribution of this work in visualizing and interpreting the empirical lifetime estimation model helps to include a comparative study between the conventional topology and the proposed topology.

After a switch fails, usually the inverter goes out of service and might cause a total loss of power delivery to the load. Therefore, the proposed design introduces the ability to use the redundant switches in the design to achieve an (N-1) system, where any single switch can fail while the inverter can maintain its operation.

1.5 Organization of the Thesis

This thesis consists of five chapters, which are organized as follows:

Chapter 2 provides an overview of failure mechanisms for power semiconductor switches. Precursors for different types of failures are presented for package and chip-related failures. Chapter 2 also overviews the temperature monitoring techniques in literature and their importance for reliability studies. Approaches to reduce the failure rate are discussed as well. Finally, Chapter 2 discusses the empirical lifetime estimation models for power switches lifetime estimation in literature.

Chapter 3 describes the development of the proposed double switch H bridge inverter topology in order to improve the system's reliability by increasing the expected lifetime of the inverter's power switches. Chapter 3 also describes the development of the novel lifetime improvement evaluation curve, highlighting the effect of $\%\Delta T_{j\_red}$ and $\%T_{jm\_red}$ on the switches' expected lifetime. Moreover, Chapter 3 provides the effect of loading conditions such as power factor and loading level on the performance of the proposed topology.

Chapter 4 shows the results of adopting the proposed double switch inverter topology and their impact on reliability. Moreover, the chapter presents comprehensive results and analysis comparing the double switch inverter topology with the conventional topology under various loading conditions.

Chapter 5 presents the conclusion on the primary contributions of the study. A few possible directions for extending the research are highlighted at the end of the chapter as well.

Chapter 2: Literature Review

This chapter reviews the importance of power converters and various power electronics switches' failure-related literature, specifically power switches in power inverters. Failure mechanisms and the precursors of failure related to power switches are presented. Temperature monitoring techniques are then discussed due to their importance in any reliability study. The mission profile of inverters in different applications requires the inverter to be adaptive to the changes in parameters such as irradiance change in Photovoltaic (PV) systems and wind speed change in wind turbine systems. Such adaptation usually comes in the form of a modulation parameter change. Thus, the effect of modulation techniques and their parameters on the power switches' degradation is discussed. Following that, a discussion on approaches to reduce the failure rate is given. Finally, lifetime estimation techniques are reported as well.

2.1 Power Converters Background

Power converters proved their importance in many applications, contributing to making power usage more efficient and versatile. This is mainly achieved by mediating between the generic power sources and the high power application to adjust the power delivery process to the appliance in a better and more efficient manner.

Power electronics converters have been in increasing demand over the last few decades, especially after the advancements in power semiconductor switches. According to previous studies [5], around 70% of the whole United States of America's use of power flows through power converters and is expected to grow to 100%.

Power converters are playing a crucial role in industrial, commercial, residential, utility, military, and aerospace applications [1]. Mainly, power converters can be found

in applications such as renewable resources, mostly PV systems, and wind turbine systems.

Renewables' share of power generation increased from 10.3% to 11.7% of the total world generation throughout the year 2020 [6] and is increasing year by year, which pushes all the elements of renewable energy systems to develop in every possible aspect, especially in terms of reliability and life expectancy.

According to PV farms' statistical data, inverters (the main power converter in PV systems) are responsible for the most unscheduled maintenance events, as shown in Figure 2.1 [7].

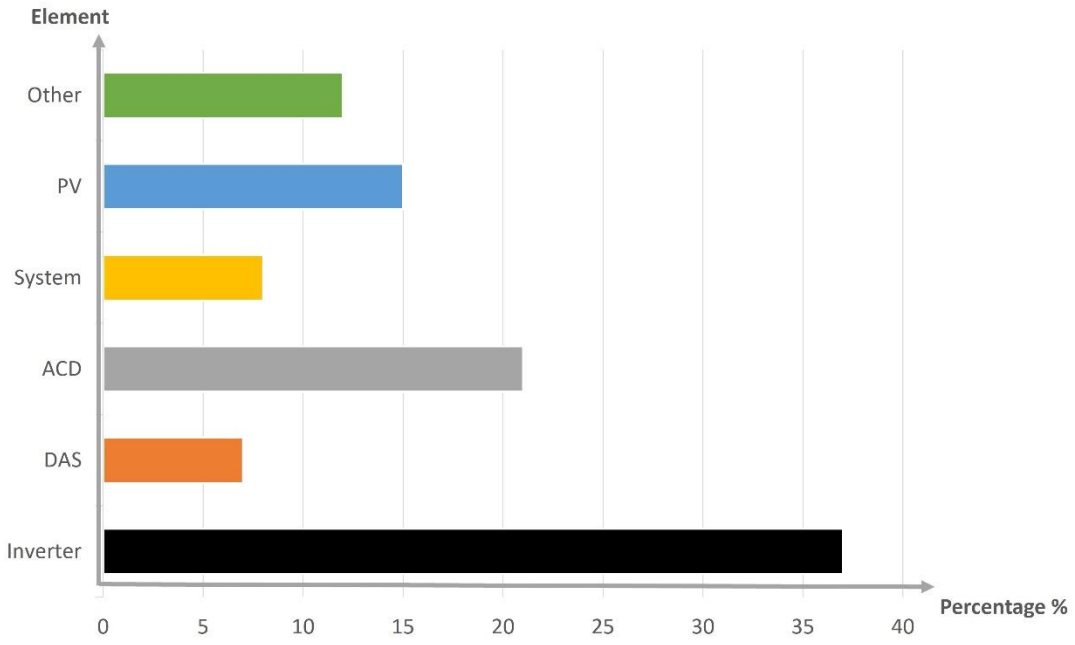


Figure 2.1: Unscheduled maintenance events in a PV farm

The same study showed that inverters were also responsible for the highest cost of unscheduled maintenance events compared to the other components of a PV system [7], as shown in Figure 2.2.

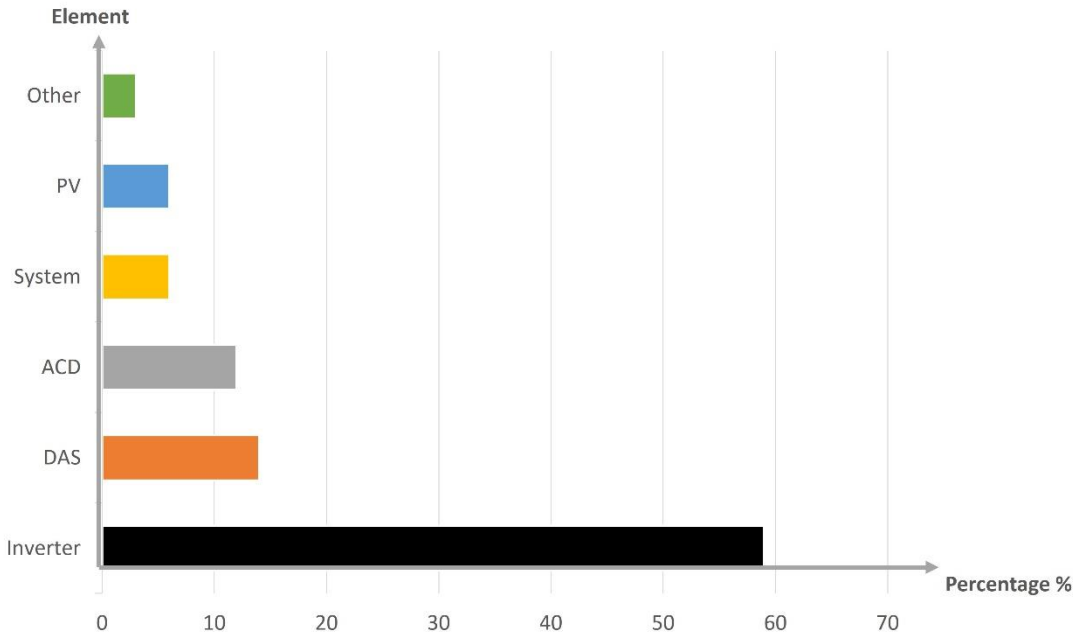


Figure 2.2: Unscheduled maintenance events cost in a PV farm

Power switches are among the inverter's common elements to fail [8]. Unfortunately, the impact of power switch failure is profound; this roots back in the fact that other inverter elements cannot play the role of power switches. Consequently, a switch failure would lead to loss of power delivery if the design did not incorporate redundancy. In addition, the failure of a power switch may lead to the failure of other internal or external components. For example, this may happen if a switch is short-circuited, causing a high current flow through other system elements, such as capacitors, terminals, batteries, and others.

2.2 Failure Mechanisms and Precursors of Failure

Several types of stress lead to the degradation and failure of electronic components. Figure 2.3 shows the common types of stress subjected to power electronics equipment and their contribution level towards the failure of such equipment. Temperature is

responsible for more than 50% of the stress subjected to power electronics devices [9]. Hence it is the dominant cause of failure among the others.

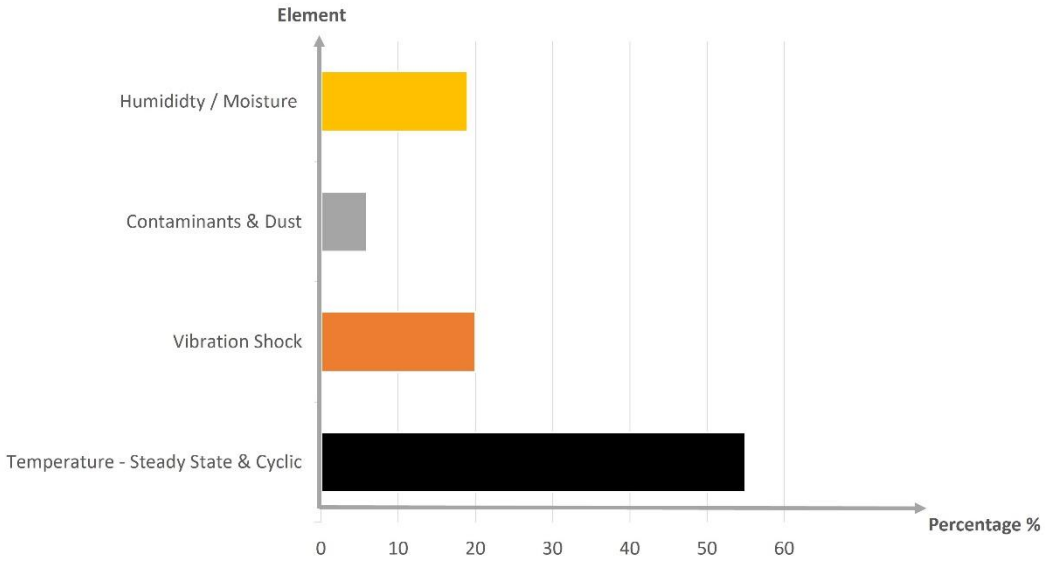


Figure 2.3: Sources of stress for electronic equipment

Failure-related studies were based on field data and statistical analysis in the past. However, researchers have been working on understanding the physical changes in electronic components in recent years. For example, the Physics of Failure (PoF) in power semiconductors was investigated in several studies to understand the reason behind power electronics failure [10]–[12].

Previous studies categorized failure mechanisms of power electronic devices into package-related failures (or extrinsic failures) and chip-related failures (or intrinsic failures) [13], [14]. The major package-related failures are bond wire failure, solder fatigue, and metallization reconstruction [15]. The major chip-related failures or intrinsic failures are dielectric breakdowns, latch-up, and electromigration [15], as shown in Figure 2.4.

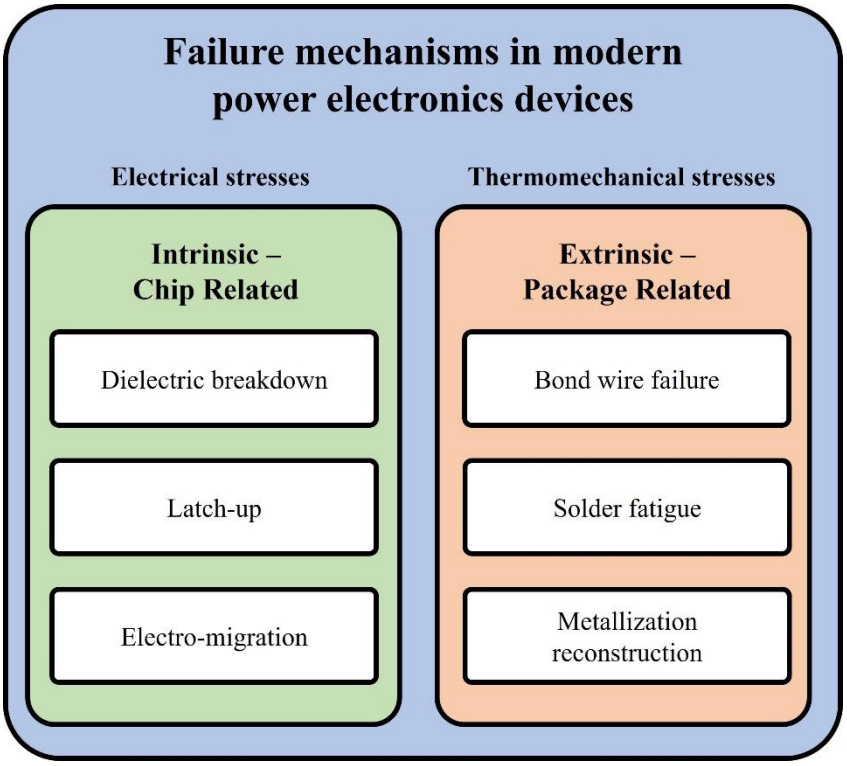


Figure 2.4: Failure mechanisms in modern power electronics devices

Package-related failures are heavily related to thermomechanical stress. On the other hand, chip-related failures are induced mainly by electrical stress such as voltage and current levels. The two failure mechanisms are briefly discussed in terms of their main inducers, thermomechanical, and electrical stresses.

2.2.1 Package Related Failures

During the usual operation of converters, the temperature of the junction swings as the principle of operation of most converters requires that the power switch must switch on and off repeatedly. In return, this drives the temperature of the switch's junction T_j to build up and cool down cyclically, causing what is called thermal cycling [15].

Thermal cycling also referred to as thermomechanical stress, can lead to different types of failure, such as bond wire failure, chip-baseplate solder fatigue, and metallization reconstruction. Figure 2.5 shows the typical structure for a multilayer power module.

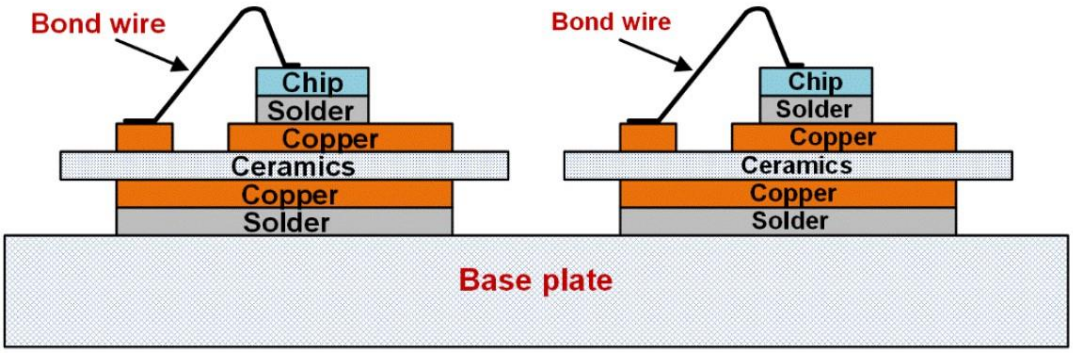


Figure 2.5: Typical multilayer structure of a power module [15]

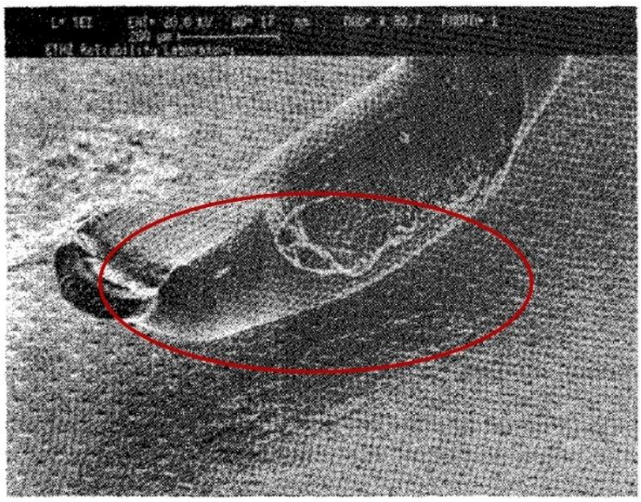
The layering of materials and bond wires characteristics affect the module's tendency to fail. Mainly, the two most occurring types of failure, namely, bond wire failure, and solder fatigue will be investigated below along with metallization reconstruction.

I. Bond Wire Failure

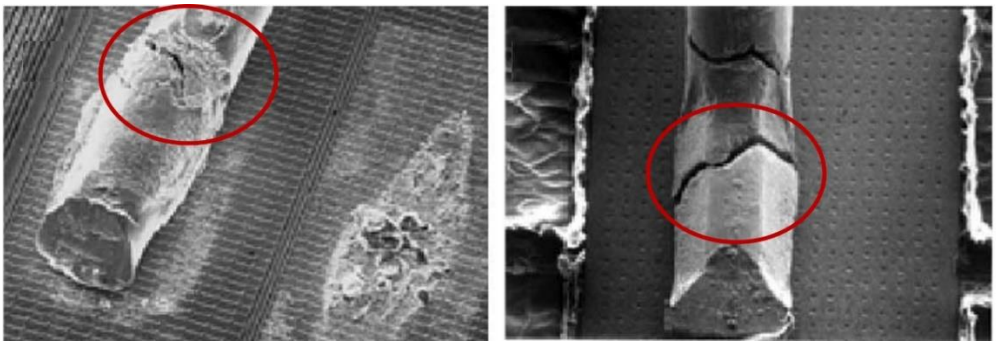
Bond wire failure is usually considered the dominant failure mechanism in power switches, particularly in Insulated Gate Bipolar Transistors (IGBTs) [16]–[18]. Bond wire failure happens in the form of a lift-off or heel crack of the bond wire, as shown in Figure 2.6, which is famously caused by thermal cycling [16], [17]. As the semiconductor heats and cools down, different materials react to temperature change differently mainly due to the difference in the Coefficient of Thermal Expansion (CTE) among different materials, as given in Table 2.1.

Table 2.1: CTE in Parts Per Million (PPM) for some of the commonly used materials in semiconductors

Material	CTE (PPM/°C)
Al	24.5
Si	3
Cu	17



(a)



(b)

Figure 2.6: Common modes of bond wire failure (a) Bond wire lift-off [12], (b) Bond wire heel crack examples [17]

II. Solder Fatigue

Referring to Figure 2.5, solder layers can be found between several layers, which implies that a failure in a solder layer might cause severe problems to the power module or even cause complete loss of the unit.

The solder layer that is most prone to fail is the layer between the ceramic substrate and the base plate, especially in the case of copper base plates [19], [20]. Thermal stress can cause the solder layer to form voids and cracks, affecting the power switch's performance. Such voids and cracks will worsen over time as the switch undergoes thermal cycling stress.[13], [14].

III. Metallization Reconstruction

Metallization reconstruction-induced failures are also one of the most frequent failures observed during the operation of power semiconductors [21]. This type of degradation is also caused by thermal cycling. The thermal cycling induced tensile and compressive stresses can exceed the elastic limit of metal plates such as aluminum, hence leading to metallization reconstruction. According to [17], such failure types can be effectively reduced by using a passivation layer.

2.2.2 Chip Related Failures

Power switches might be subjected to electrothermal or electrical stresses during normal operation. Commonly, electrical stresses cause chip related failures such as dielectric breakdown [14], [15], electro-migration [14], [15], and latch-up [15].

A. Dielectric Breakdown

Dielectric breakdown happens when an electric field with sufficient strength starts a current channel in a supposedly insulating medium [22]. For example, in the case of the IGBTs, the breakdown might happen between the Gate-Collector or between the Gate-Emitter.

As illustrated in Figure 2.7, a dielectric breakdown can be in the form of a catastrophic breakdown or Time-Dependent Dielectric Breakdown (TDDB). The catastrophic breakdown usually happens due to junction overvoltage or excessive heating in some cases [23]. In contrast, as the name implies, TDDB comes in the form of degradation over time [23], which is caused by chronic defect accumulation in the silicon oxide insulator [24]. Usually, TDDB can come in the form of gate oxide breakdown at relatively low electric fields after a long period of operation [25].

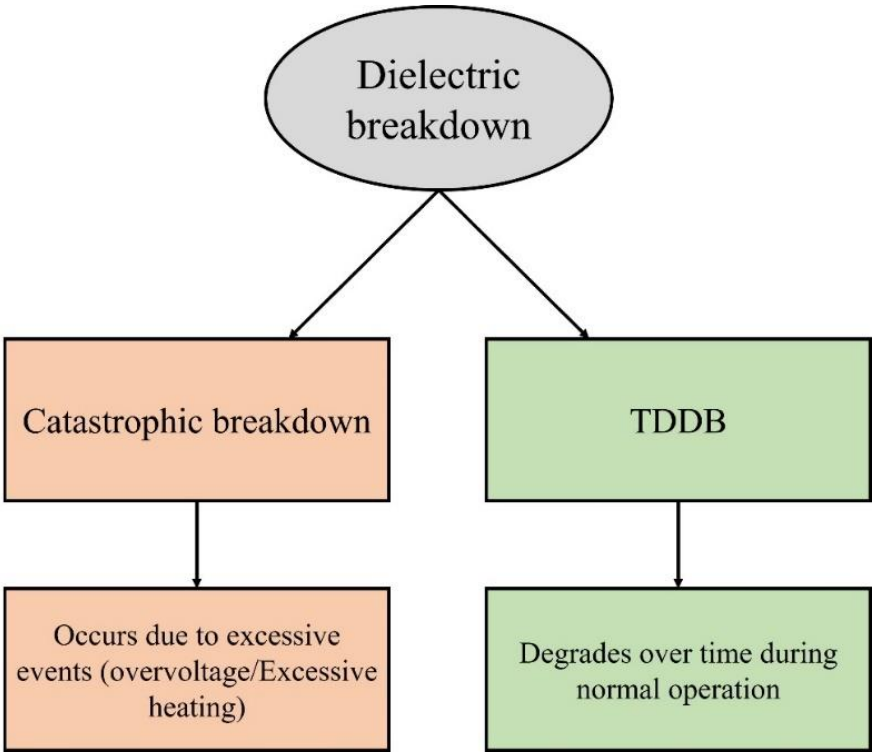


Figure 2.7: Dielectric breakdown types

B. Latch-Up

Latch-up failures are in the form of gate control loss of the power switch. This failure can be caused by high operating temperatures accompanied by high dv/dt [26], [27]. Such dv/dt interacts with the switch's parasitic elements, causing the switch to latch-up and stay on even while the gate circuitry is acting to turn the switch off. This can lead to high currents flowing through the switch, causing the switch and probably other components to fail [28].

C. Electro-Migration

Electro-migration is an atomic migration of metals between silicon interconnects due to high current densities over the long term, especially for devices with small contact areas [9], [22]. Such migration can lead to the formation of voids, which raises the ON resistance of the device and can cause open circuit failures in the long term. However, it is one of the failure modes rarely observed in power electronics because power electronic devices are usually built with large contact areas.

Table 2.2 summarizes the main failure mechanisms for power semiconductors and shows that thermal cycling induces the most occurring failure mechanisms.

Table 2.2: Comparison of main failure types in power semiconductor switches

Failure	Failure type	Primary inducer	Frequency of occurrence
Bond wire failure	Package related	Thermal cycling	Highest
Solder fatigue	Package related	Thermal cycling	
Metallization reconstruction	Package related	Thermal cycling	High
Dielectric breakdown - catastrophic	Chip related	Sudden electrical events	Unpredictable
Dielectric breakdown - TDDB	Chip related	Electric fields (High voltages)	Moderate
Latch-Up	Chip related	High dv/dt	
Electro-Migration	Chip related	High current density	Lowest

Intuitively, the lifetime of a device is limited by the first occurring failure mechanism; hence, the concentration of the work must be directed to relieve the primary inducer of the most occurring failures in the field – in the case of power converters: thermal cycling.

2.2.3 Degradation Indicators and Precursors of Failures

The study of power switches' degradation is critical because it enables to estimate of their lifetime expectancy for a given application's mission profile. In addition, it allows sensing a probable upcoming failure before it happens. Prevention from a switch failure is necessary to avert a sudden loss of power delivery. Furthermore, it enables the operator to schedule a maintenance event rather than dealing with unpredictable events that are more costly and bothersome.

During the degradation period, precursors to failure are simply some measurable variables that indicate how healthy the switch is. Also, they provide information regarding which type of failure to expect and when it will happen. Typically, several degradation mechanisms may influence a degradation indicator [29]. Conversely, one degradation mechanism can influence various indicators. Hence, it is insufficient in most cases to use a single parameter to monitor degradation [30].

Figure 2.8 provides examples of degradation mechanisms and corresponding indicators. As mentioned earlier, a degradation mechanism might be indicated by more than one measurable variable (indicator). A great example is the gate oxide degradation, which might be indicated by a change in the forward voltage drop at high currents, a shift in the switch's threshold voltage, or a gate leak current increase.

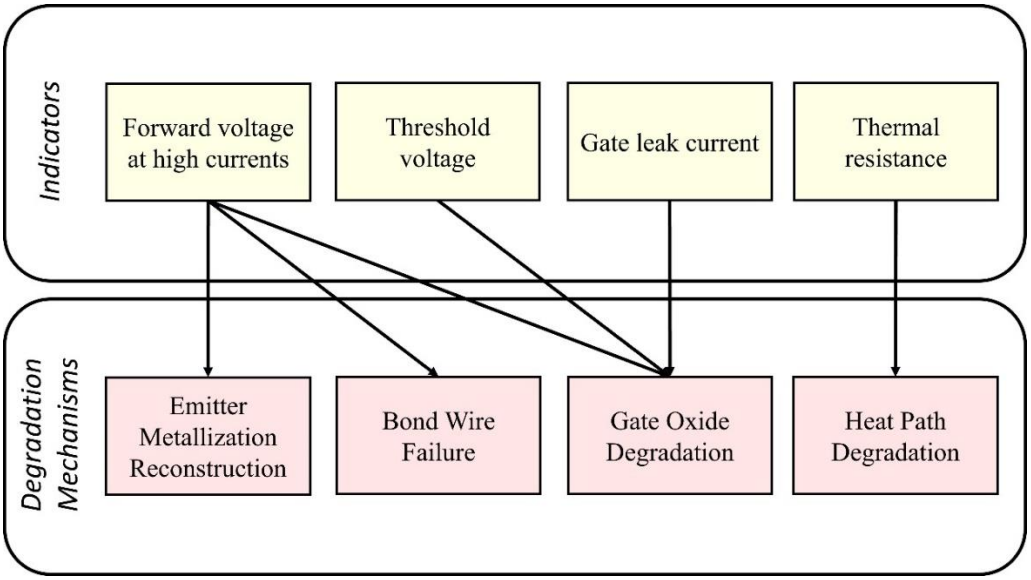


Figure 2.8: Common degradation indicators

Meanwhile, a degradation indicator might be induced by several degradation mechanisms. For example, the change in the switch's forward voltage drop at high currents can indicate emitter metallization reconstruction, bond wire failure, or gate

oxide degradation. For this reason, proper condition monitoring requires the consideration of multiple indicators altogether.

It is worth noting that chip-related failures are usually due to overstress conditions; hence they can hardly be forecasted accurately by degradation indicators [31]. Nevertheless, monitoring the degradation indicators can reveal the switch's health and hence how vulnerable the switch might be to fail in an overstress condition [30]. This implies that monitoring the degradation indicators can be beneficial for predicting both chip-related and package-related failures.

Taking the case of IGBTs bond wires' failure as an example, the forward voltage drop across the collector-emitter terminals (V_{ce}) witnesses a sudden increase in case of a bond wire lift-off. This event is illustrated in Figure 2.9 [32].

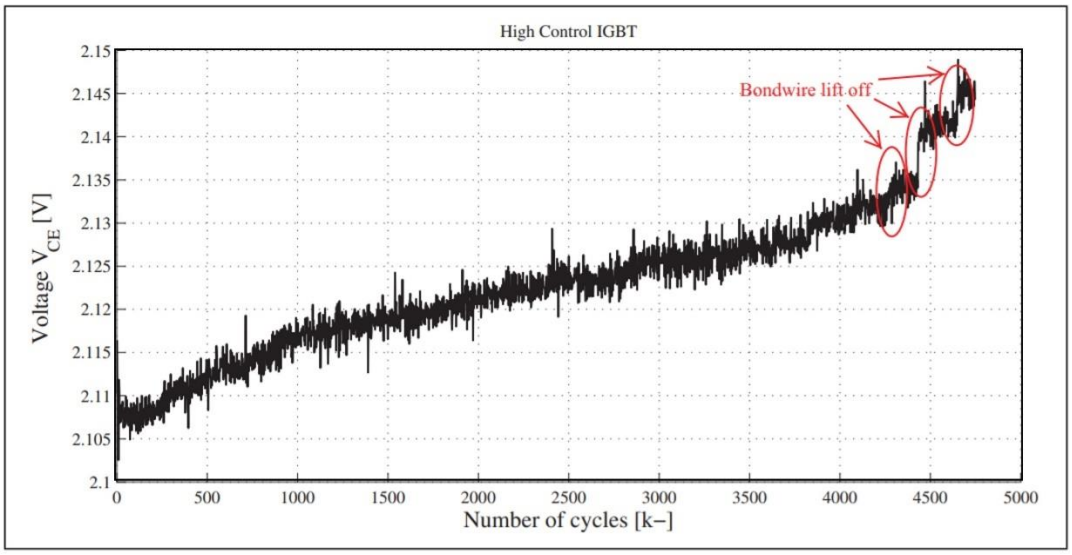


Figure 2.9: IGBT's forward voltage drop variation due to bond wire lift-off [32]

Due to the increased current flowing through the remaining bond wires, a bond wire lift-off causes extra stress on the remaining bond wires. This can be realized from the domino effect shown in Figure 2.9, where two additional bond wire lift-offs occurred

shortly after the first one. This domino-like effect depends on the value of current flowing through the IGBT and might result in an out-of-service IGBT.

2.3 Temperature Monitoring

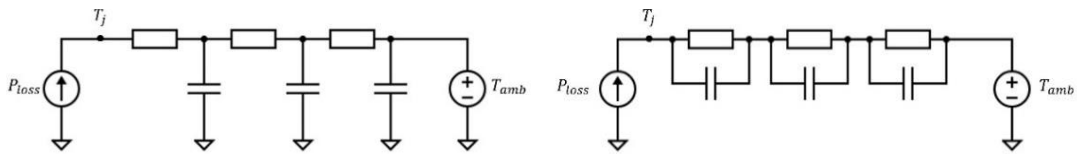
One of the most important steps required to evaluate power electronic devices' lifetime and reliability is temperature monitoring. Generally, temperature monitoring can be grouped into three types: temperature sensing, thermal estimators, and thermal observers, all well-reviewed in [33].

Temperature sensing is one of the commonly used temperature monitoring methods, usually done by utilizing on-die-sensors as suggested in [34] or via Temperature-Sensitive Electrical Parameters (TSEP) as illustrated in [35]. In addition, the authors in [30] evaluated the implementation issues of temperature sensing.

Meanwhile, as the name implies, thermal estimators are meant to estimate temperatures based on the device's losses rather than measuring temperatures. A thermal estimator uses open-loop electrothermal models to estimate the junction temperature based on measured or calculated losses [33]. This makes thermal estimators the simplest among the three types of temperature monitoring. Although it does not provide an actual reading of the temperature, it is widely accepted in the field. Crucially, thermal estimators require accurate loss calculation models to obtain the instantaneous losses, which are fed to the electrothermal model to estimate the junction temperature. Thermal estimators' models are commonly constructed using RC chains. The most famous RC models used are Cauer and Foster models, shown in Figure 2.10. Thermal estimators can be used for implementing active thermal control as proposed in [36]. In another study [37], thermal estimators were also used to monitor the power devices' junction temperature in 3-phase power converters.

Lastly, thermal observers combine the two methods mentioned earlier, namely, thermal sensing and thermal estimators. Sophisticated thermal observers can be used in power switches' health diagnoses purposes, especially in critical applications where reliability is of most concern and applications where the health of components is challenged by harsh environments [37].

As discussed earlier in previous sections, the temperature is a critical factor in the performance and reliability of electronic devices, specifically semiconductors. In addition, wear-out mechanisms such as die-attach degradation and bond wire failure rely heavily on the average temperature level and temperature fluctuation. Hence, obtaining the junction's temperature is crucial.



a) b)

Figure 2.10: The two standard thermal network models are a) Cauer network, and b) Foster network

The use of thermal estimators is the most general approach from the categories above due to their simplicity in contrast with thermal observers and temperature sensing approaches. Cauer and Foster networks as thermal estimator models are attractive because of their flexibility. They can comprise as many RC chains as desired, depending on the accuracy/complexity trade-off of the estimation. The final RC network represents the thermal impedance of the system, with each RC chain representing a single time constant. The more RC chains are sequenced in the network,

the more accurate the thermal response of the network gets at the expense of complexity.

The transient thermal response to a step power input is commonly used to describe the package's thermal characteristics. The derivative of the input step function is an impulse which is usually referred to as the system's response [38], [39].

Various approaches were proposed to find the optimal RC structures, such as the sequential forward selection algorithm for a micropyrotechnic actuator [40], a thermopile-based IR sensor [41], and the reduced dynamic thermal models from the time constant spectra of transient temperature responses [42].

As opposed to RC structures optimization, the RC values of these structures are usually obtained using curve fitting techniques, for example, nonlinear least-squares optimization, which was used in [40] to extract a dynamic multiport thermal compact model with the help of genetic algorithms. Furthermore, a boundary-independent Dynamic Compact Thermal Model (DCTM) was extracted using the same technique in [41], which was then applied to a thermopile-based IR sensor.

Another curve fitting technique is called recursive least square identification [43]. This technique recursively finds the coefficients R and C that minimize a weighted linear least-squares cost function obtained from the Transient Thermal Impedance Curves (TTIC) provided in the datasheets. Figure 2.11 summarizes the parameter extraction technique used in [43].

In [44], a study was done to predict the transient thermal behavior of a handheld telecommunication device using a technique called linear regression curve fitting. The values of R and τ (time constants) of the thermal model were extracted based on the

method with the help of superposition. Figure 2.12 explains the process where the thermal response for a single pulse is obtained, and then superposition is adopted to extract multiple thermal responses for multiple pulses. At last, adding these responses together results in the overall thermal response. However, it is worth noting that this approach requires the system to reach steady-state operation to estimate the junction temperature at a given instance.

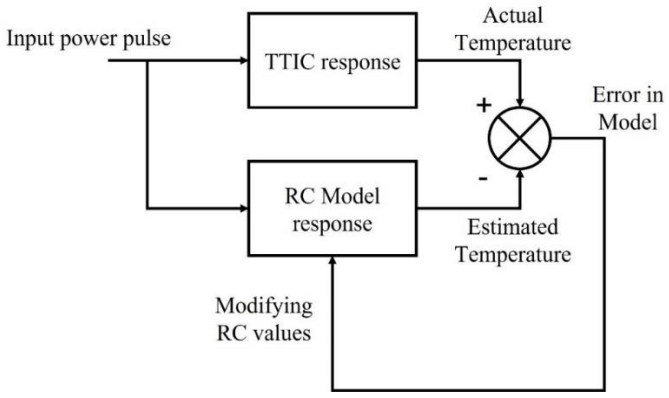


Figure 2.11: recursive least square used in [43]

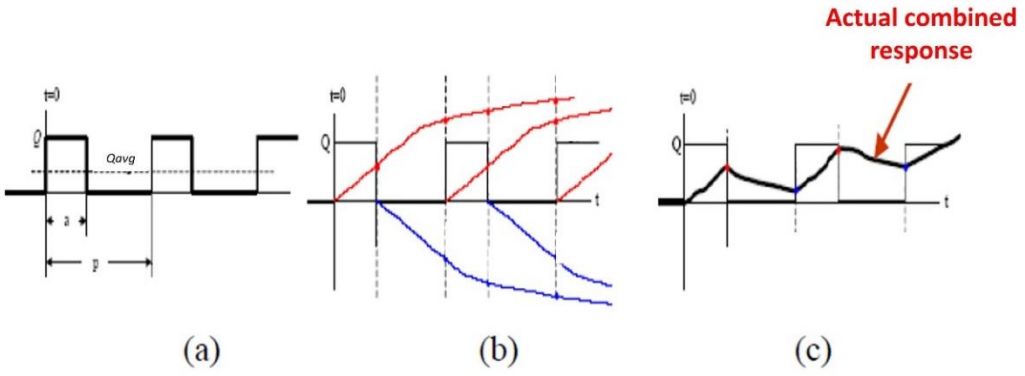


Figure 2.12: Linear regression curve fitting results for (a) square pulses as input to obtain the Transient thermal response, (b) individually per pulse (heating and cooling), and (c) the actual combined thermal response

Cauer networks have the advantage that each RC link represents a physical layer in the component, and each node's voltage represents the temperature of a point in the physical structure of the power switch. The temperature access points start with the chip's junction temperature and ascend to the case temperature via chip solder, substrate, and substrate solder up to the case. Then, additional RC links representing the heatsink and interface between the case and heatsink can be added to obtain the total impedance from junction to ambient (Z_{j-a}). Finally, feeding the instantaneous losses into the finalized network would yield the estimated instantaneous temperature at any layer of the system [36]. Cauer networks are usually used when a Finite Element Analysis (FEA) is performed to obtain the thermal impedances [30]. However, this can be a bit challenging to get very accurate models unless relatively full knowledge of the intrinsic composition of the power semiconductor is available.

In contrast to Cauer networks, Foster networks lack the physical meaning that Cauer networks offer, but they can be extracted easier than Cauer networks [39]. Cooling curves are usually analyzed to obtain the RC coefficients for Foster networks, which is more straightforward than FEA [45]. The extracted cooling curves can describe the thermal behavior, including heatsinks and interfaces between several system components. It is worth noting that the thermal impedance curves provided in transistors' datasheets are usually Foster network-based, as shown in the curve in Figure 2.13. This way of presenting the thermal impedance is helpful because it is not constrained by knowing the complex internal structure of the semiconductor [45], which adds in favor of Foster networks utilization.

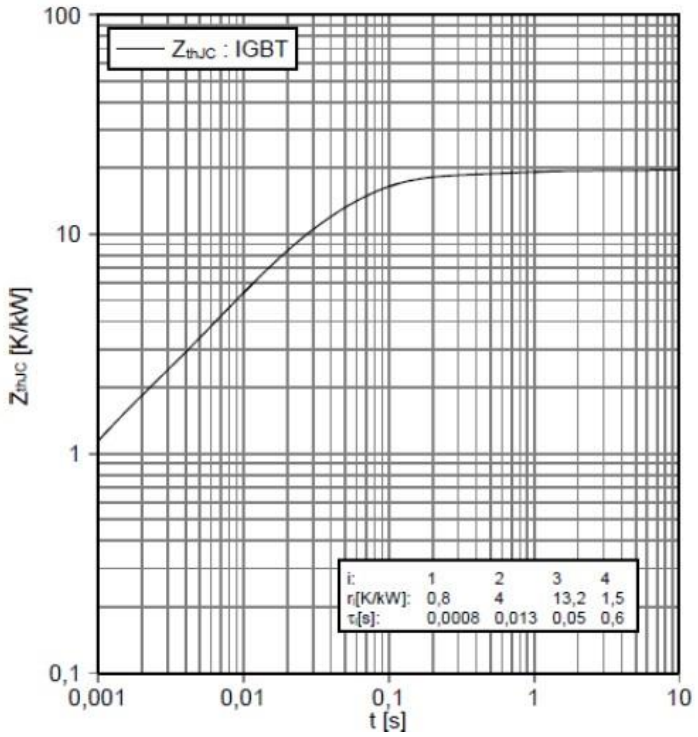


Figure 2.13: Example of how thermal impedance is given in datasheets based on a Foster network configuration [45]

The transformation between Foster and Cauer networks is possible [39], [45], [46]. Hence, a Foster network can be extracted using recorded cooling curves, and then it can be transformed to the desired Cauer configuration as discussed in the literature [47].

Additionally, studies like [48] worked on developing the thermal model to mimic the actual thermal behavior better by including the effect of temperature-dependent variables that affect the system's performance and affect the junction's temperature. Other studies focused on producing a physics-based thermal model using the FEA approach [11] to retrieve a better customized thermal model. However, even though these modified models provide more accurate results than conventional models, their complexity reduces their popularity in systems beyond research [49].

The use of heatsinks lessens the junction's temperature and affects the thermal spreading among the layers of the module. Hence, it is advised in literature [45] to use the complete structure with the heatsink when extracting the thermal model of the system rather than combining separately-extracted thermal models. This reduces the number of setups and provides a more accurate representation of the overall thermal impedance from junction to ambient (Z_{j-a}). , as shown in Figure 2.14.

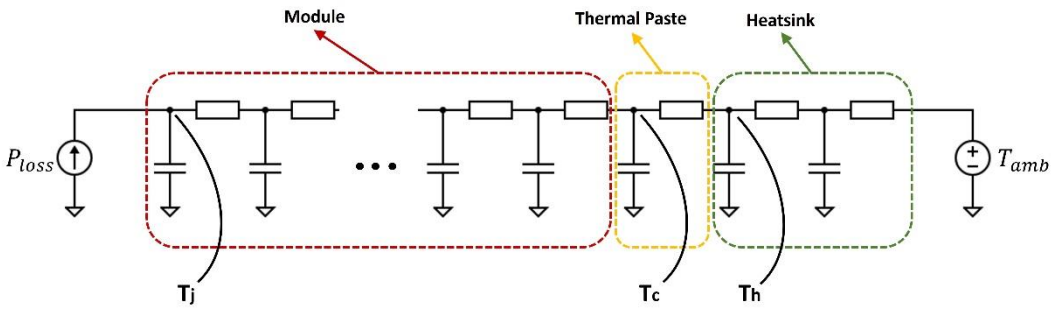


Figure 2.14: Full Cauer Network from Module to Heatsink

As stated above in Figure 2.10 and Figure 2.14, the driving current of RC networks represents the power loss in the device. Hence a proper calculation/measurement of the overall power loss is necessary.

2.3.1 Power Losses in Power Switches

Power losses in power switches are significant to understand as they are the primary source of thermal stress. Power losses are commonly classified into two types, namely, conduction losses P_{cond} and switching losses P_{sw}. Both types occur when a voltage and current overlap simultaneously. Power loss can be expressed as:

$$P = V \cdot I \tag{2.1}$$

A. Conduction Losses

Conduction losses result from the current flow through a conductive path's resistance, i.e., through the semiconductor's ON resistance. Conduction losses can be calculated as follows:

$$P_{cond} = R_{on} \cdot I_{RMS}^2 \tag{2.2}$$

Where (R_{on}) is the ON resistance of the device when a certain amount of current (I_{RMS}) is flowing through the device.

The calculation of conduction losses is straightforward, but it can be further extended to include some variables, such as a temperature-dependent ON resistance as illustrated in [50].

B. Switching Losses

Switching action in power semiconductors results in an overlap between voltage and current caused by the device's switching nature. For instance, when a switch turns on, the voltage does not fall until the current reaches its final value, and vice versa regarding the switching off. The area of overlap is well illustrated in Figure 2.15. Nevertheless, the concept of switching power losses still follows the concept of power loss occurrence whenever current and voltage are present simultaneously, as per Equation 2.1.

$$P_{sw} = \frac{V_{DS/CE} \cdot I_{D/C}}{2} \cdot (T_{on} + T_{off}) \cdot f_{sw} \tag{2.3}$$

Equation 2.3 is usually used to calculate the power loss due to switching either in a MOSFET (V_{DS}/I_D), or an IGBT (V_{CE}/I_C), where T_{on} and T_{off} are the durations of turning on and off events, respectively.

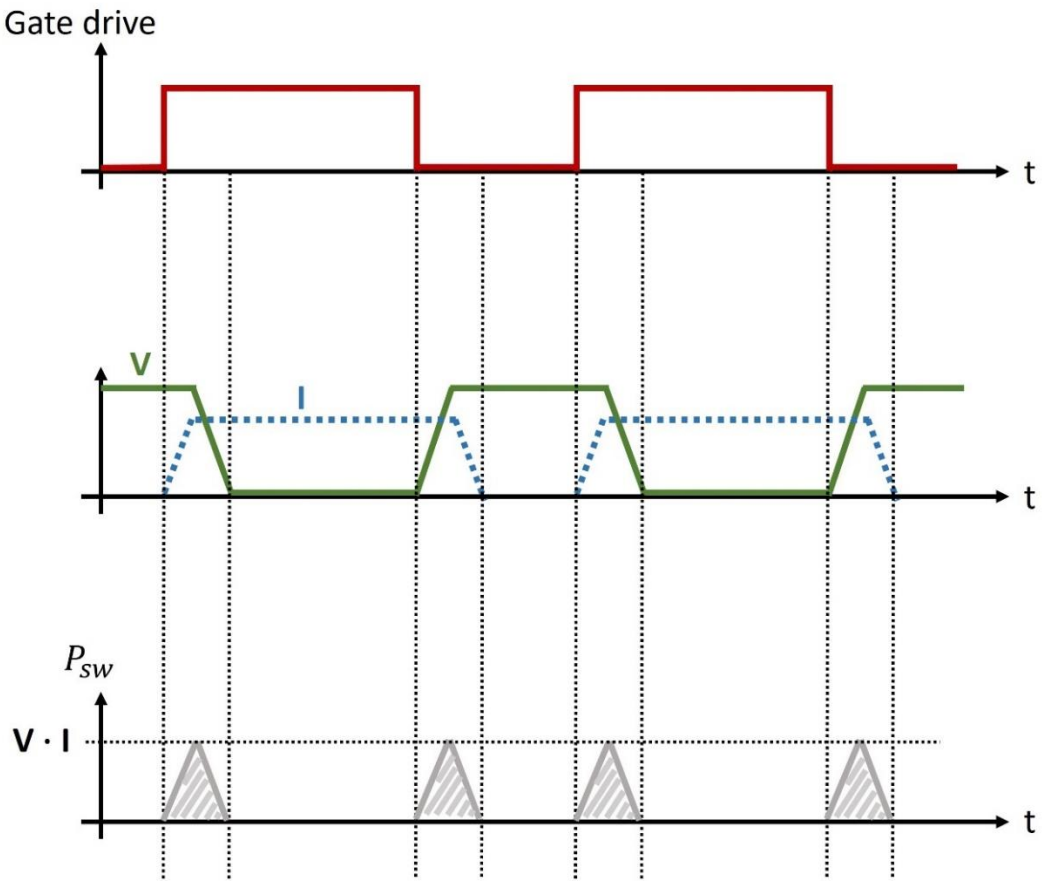


Figure 2.15: Switching action in power switches

Figure 2.15 illustrates the simplified switching action in power switches. The area underneath the grey triangles represents the lost energy. The rate at which this energy is lost per second represents the average power lost.

For temperature estimation purposes, one might be more interested in obtaining the instantaneous power loss rather than an average value because the temperature rises and falls based on the instantaneous change in the power lost in the device. However, in reality, the rise and fall of temperature do not happen linearly. However, they have a nonlinear nature depending on the parasitic element of such semiconductors, including capacitances and inductances.

Usually, switching losses are measured practically using "double pulse" testing [45]. However, other studies [51] better estimated the power loss due to switching by adopting the "opposition method". This measurement is essential to extract the instantaneous junction temperature T_j. Furthermore, in [52], ΔT_j was obtained for several modulation techniques based on the instantaneous losses calculated using a modified version of the opposition method.

2.4 Effect of Modulation Techniques on Power Switch Degradation

In practice, different converters operate in different conditions that the system is usually built to accommodate. For example, wind turbine converters are programmed to adapt to the change in wind speed and any other known variation that could affect its performance. Solar PV systems are also built to adapt to irradiation changes and partial shading. Intuitively, such converters' adaptation comes in the form of a change in PWM parameters. This adaptation requirement might create a more aggressive/destructive thermal stressing leading to unforeseen accelerated degradations or failures. The relation between thermal stress and PWM techniques will be discussed in this section.

Mainly, the degradation of a semiconductor switch is highly influenced by the temperature swing it experiences (ΔT_j), referred to as power cycling or thermal cycling. The leading causes behind thermal cycling are the variation of instantaneous losses throughout the operation and the changes in the ambient temperature. The effect of the ambient temperature on ΔT_j is out of the scope of this study. In contrast, the impact of modulation techniques on the instantaneous losses and ΔT_j will be reviewed in this section.

The semiconductor's thermal cycling intensity can differ for different modulation-related operational parameters. Some of the most impactful ones are illustrated in Figure 2.16.

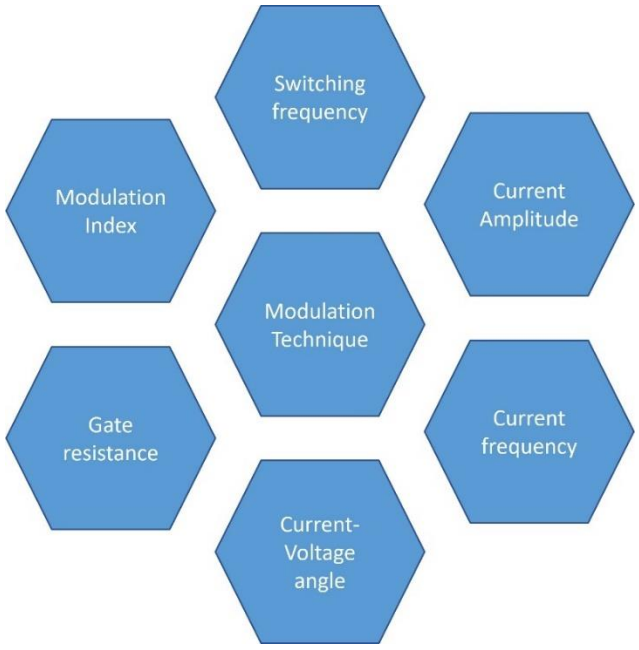


Figure 2.16: The examined operational parameters affecting thermal cycling

The study [50] discussed multiple modulation techniques used for Voltage Source Inverters (VSIs). Building on that, the authors of reference [50] put a great effort into studying the effect of these different modulation techniques on thermal cycling represented by ΔT_j. The modulation techniques covered in [53] include various Continuous PWM (CPWM), such as Sinusoidal Pulse Width Modulation (SPWM) -(unipolar)-, Space Vector Pulse Width Modulation (SVPWM), third harmonic injection pulse width modulation THIPWM, as well as different Discontinuous PWM (DPWM) including DPWMMIN, DPWMMAX, DPWM0, DPWM1, DPWM2, DPWM3, and from [54] PWMBC. Those mentioned above, continuous and discontinuous modulation techniques revolve around the idea of injecting additional

waveforms to the conventional modulating sinusoidal waveform. They are described in [55] and are shown in Figure 2.17. Each modulation technique was individually investigated while varying the operational parameters given in Figure 2.16 to find the influence of the various operating conditions on ΔT_j.

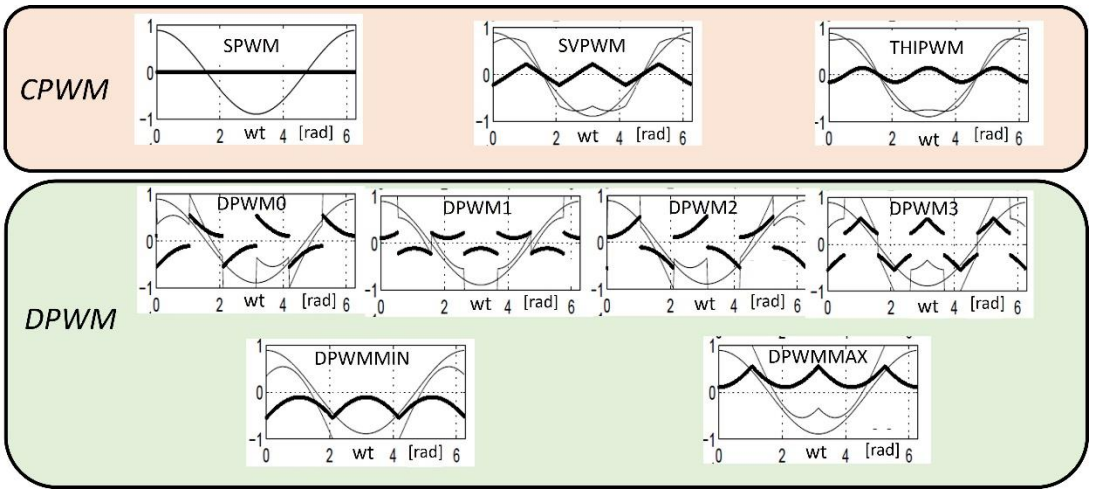


Figure 2.17: The studied Continuous and Discontinuous modulation techniques

The junction temperature can be estimated based on calculating the instantaneous power loss of the switches, which can be fed to the electrothermal model network and deduce the instantaneous junction temperature. In return, this can easily show an estimate of the behavior of ΔT_j and even different temperatures for different points in the layout.

The study [50] provided comprehensive results illustrating the relationship between ΔT_j with the parameters for different modulation techniques shown in Figure 2.18.

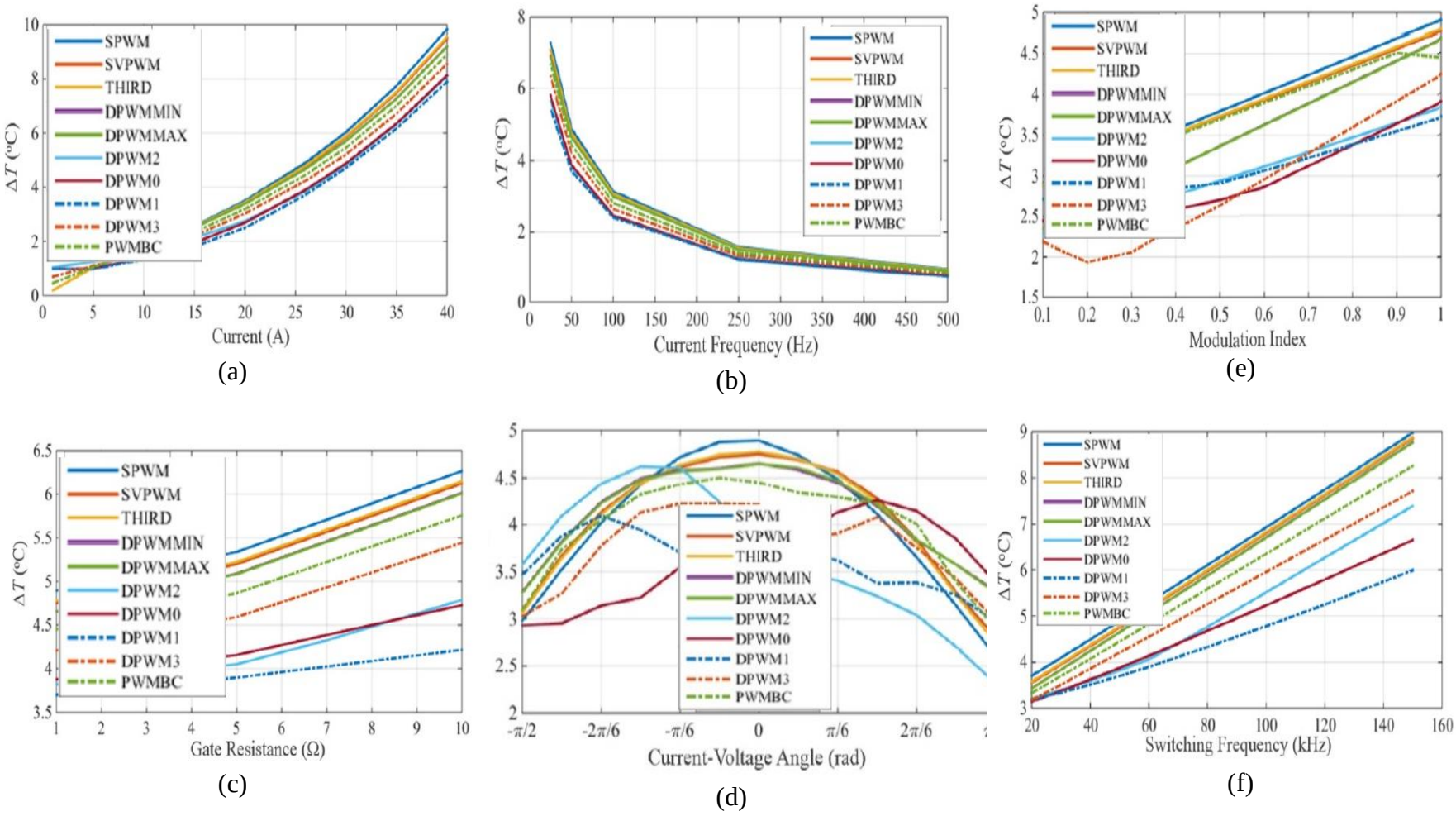


Figure 2.18: ΔT_j with respect to several operating parameters: (a) Current value, (b) Current frequency, (c) Gate resistance, (d) Current-Voltage Angle, (e) Modulation index, and (f) Switching frequency [50]

Regarding the ten modulation techniques mentioned above, Figure 2.18 (a), (c), (e), (f) generally show an increase in ΔT_j with the increase of current, gate resistance, modulation index, and switching frequency, respectively. While Figure 2.18 (b) shows a decrease in ΔT_j as the frequency of the current increases, and Figure 2.18 (d) describes the relation between ΔT_j with the current-voltage angle, which shows symmetry around the angle 0° (unity displacement power factor), with it being the worst-case scenario in terms of this parameter.

In another study [56], various Impedance Source Inverters (ISI) or (quasi-Z-source inverter qZSI) modulation techniques were investigated comparatively in terms of thermal stresses and cycles to failure.

The studied qZSI modulation techniques in [56] are:

- Maximum-Boost Space Vector (MBSV).
- Maximum-Boost Modulation (MBC).
- Maximum-Boost Modified Space Vector (MBMSV).
- Maximum-Constant-Boost (MCB).
- Simple-Boost techniques such as (ZSVM6, ZSVM4, and SBC).
- Simple-Boost Modified Space Vector (SBMSV).

These modulation strategies are illustrated in Figure 2.19.

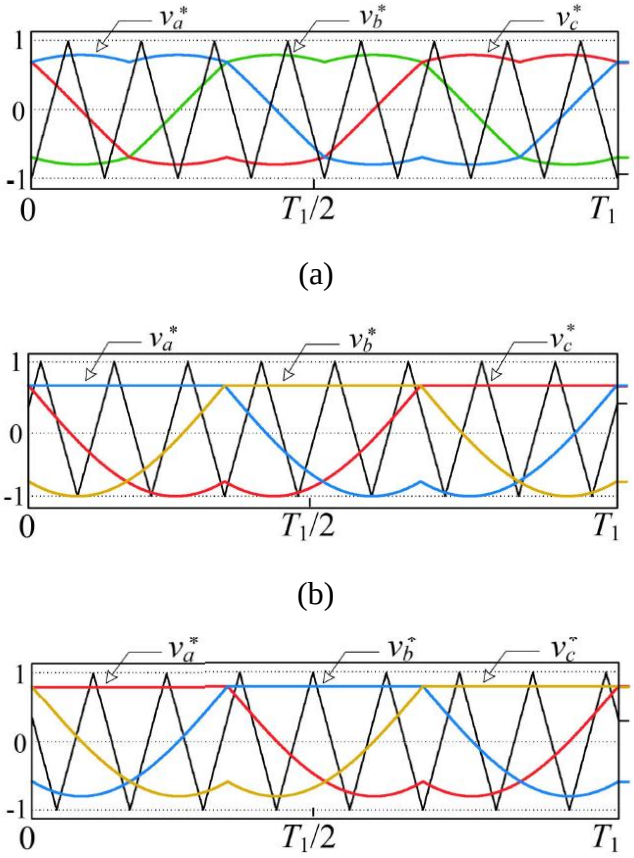
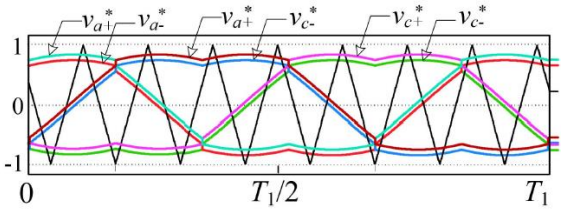
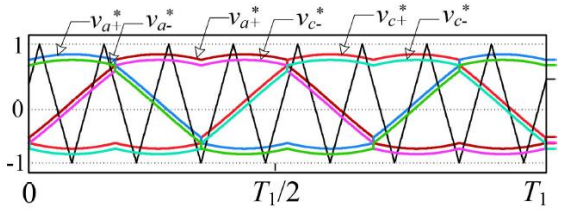


Figure 2.19: Several modulation strategies for qZSI: (a) MBSV, (b) SBMSV, (c) MBMSV, (d) ZSVM6, (e) ZSVM4, (f) SBC, (g) MBC, and (h) MCBC [56]



(d)



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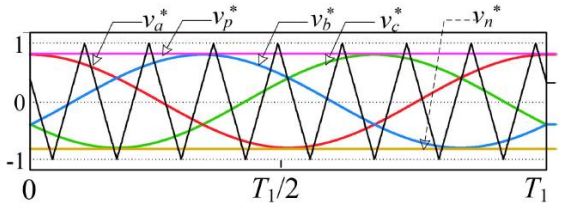

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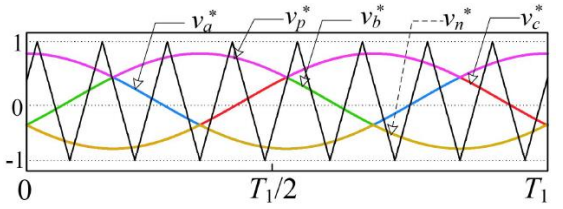
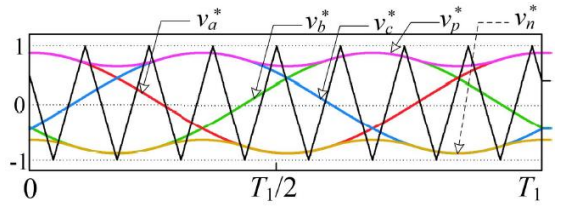


(g)



(h)

Figure 2.19: Several modulation strategies for qZSI: (a) MBSV, (b) SBMSV, (c) MBMSV, (d) ZSVM6, (e) ZSVM4, (f) SBC, (g) MBC, and (h) MCBC [56] (continued)

The thermal stress (T_{jm} and ΔT_j), as well as the cycles to failure for all of the above modulation techniques, are summarized in Table 2.3.

Table 2.3: Junction temperatures and cycles to failure for the studied modulation techniques in [56]

		T_{jm}°C	ΔT_j°C	N_f
MBSV		61.9	1.293	1.603×10^{14}
SBMSV	Positive side switch	53.3	2.229	1.811×10^{13}
	Negative side switch	80.5	2.159	3.932×10^{12}
MBMSV		60.7	1.387	1.216×10^{14}
ZSVM6		110.9	2.475	3.974×10^{11}
ZSVM4		110.8	2.377	4.895×10^{11}
SBC		122.4	2.577	1.885×10^{11}
MBC		104.4	1.531	6.163×10^{12}
MCBC		113.6	2.304	5.004×10^{11}

Both studies [50], [56] proved the impact of modulation on the degradation rate and cycles to failure (N_f) of the power switches in inverters. Interestingly, some modulation techniques in [50] had close average overall losses but substantially different N_f. This will be further examined in Section 2.5.

2.5 Approaches to Reduce the Failure Rate of Switches

Fail rate/Lifetime of power IGBTs/MOSFETs are terminologies to describe their reliability. Both are determined based on the degradation of power semiconductors

discussed throughout several subsections in Section 2.2. In addition, appointed by many studies, the focus to improve the fail rate of power switches is based on the junction temperature, explicitly reducing the cycling stress caused by ΔT_j as much as possible, like the work done in [57]–[60].

2.5.1 Modulation

Not many studies were oriented towards improving reliability from the thermal point of view by tweaking the modulation technique or adjusting its parameters. One of the studies [4] investigated the switching frequency adjustment to reduce thermal cycling. Another study [61] investigated the switching frequency adjustment and limiting the supplied current to obtain a less thermal cycling effect on switches and, therefore, achieve better system reliability. What is repellent about both approaches is that they intervene in the operation of the inverter. For example, the first study proposes reducing the switching frequency; this may increase the output waveform's Total Harmonic Distortion (THD) to unacceptable levels for some applications. On the other hand, the second study proposes to limit the output current, which constrains the power limit of the converter.

Regarding studies [50], [56], the authors did not propose a new modulation technique to reduce thermal cycling but rather performed a comparative study. Nevertheless, their efforts can be taken as a guideline to improve the inverters' reliability by changing the modulation technique for some applications.

An interesting observation from [50] is that two mirrored instantaneous losses waveforms with the same average losses and peak-to-peak losses resulted in significantly different temperature responses, as shown in Figure 2.20.

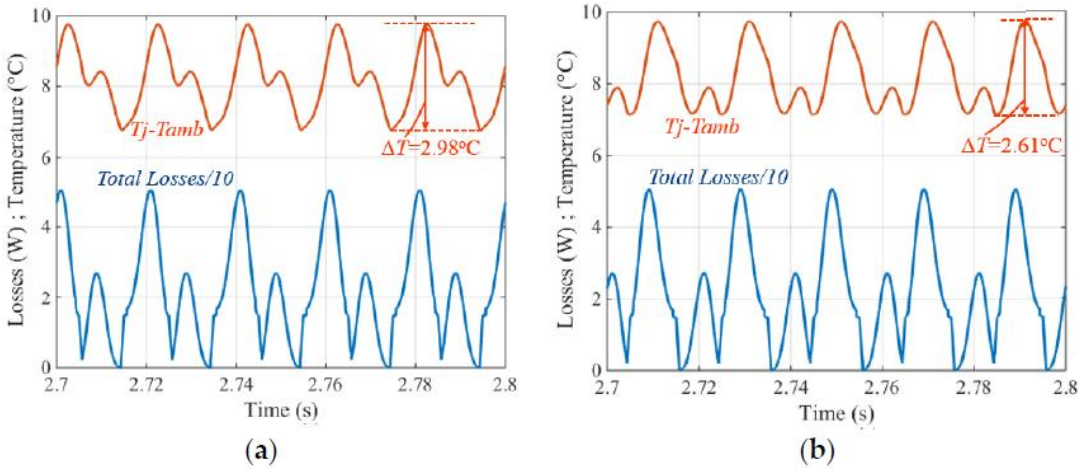
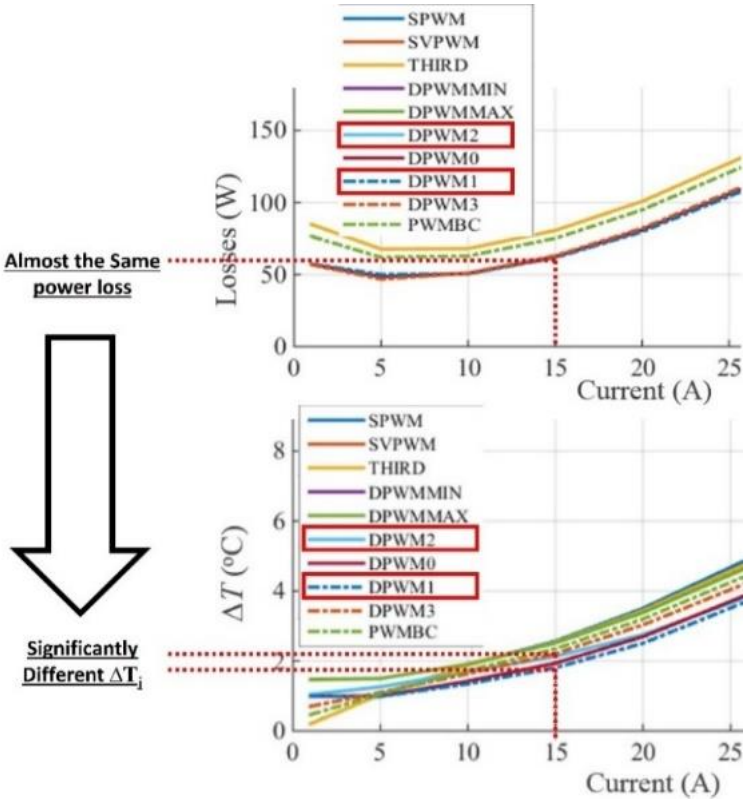


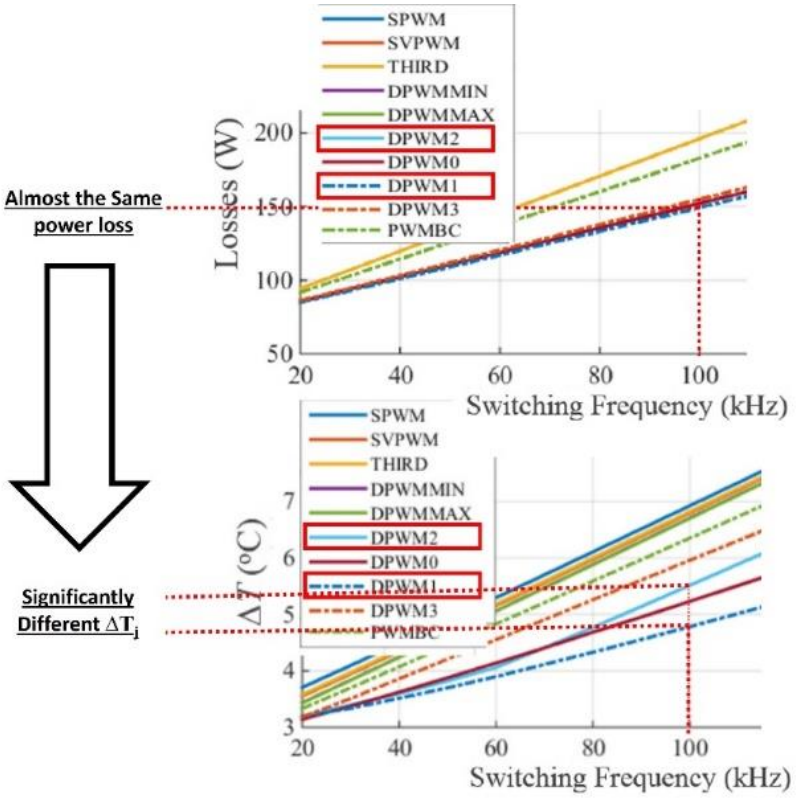
Figure 2.20: Instantaneous losses (bottom curves) and junction temperature variation (upper curves) [50]

The ΔT_j difference between cases (a) and (b) in Figure 2.20 can lead to a substantial difference in cycles to failure between the two scenarios. A query arises about which feature of the power loss waveform most influences ΔT_j. Also, this gives a hope that more modulation techniques can emerge in the future in favor of power switches' reliability without negatively impacting or intervening in the operational aspect of the inverter.

Consequently, Figure 2.21 analyzes the (ΔT_j / current) and (ΔT_j / switching frequency) curves while comparing the two modulation techniques DPWM1 and DPWM2 performances. The comparison reassures that the average power loss of a modulation technique is not an adequate indication of its resultant thermal cycling effect.



(a)



(b)

Figure 2.21: Different ΔT_j for DPWM1 and DPWM2 at operating points with almost the same average power loss at (a) 15 Amps current and (b) 100 Khz switching frequency

In another study [62], the mission profile of a motor drive shown in Figure 2.22 was considered to examine the effect of the PWM method on the upper and lower switches' temperature in an inverter.

The same study proposed an asymmetric modulation technique shown in Figure 2.23 to improve the lifetime expectancy. This asymmetric modulation technique is meant to reduce the losses on the most stressed switch among the high and low side switches depending on the application used in [62].

As Figure 2.24 (a) clearly shows, the lower switch in one of the converters' legs is stressed more than the higher switch of the same leg when SVPWM is applied. Hence, the lifetime of the converter is constrained by this switch's health. Furthermore, Figure 2.24 (b) shows the impact of their proposed asymmetric modulation method on the temperature of the lower switch compared to the conventional SVPWM.

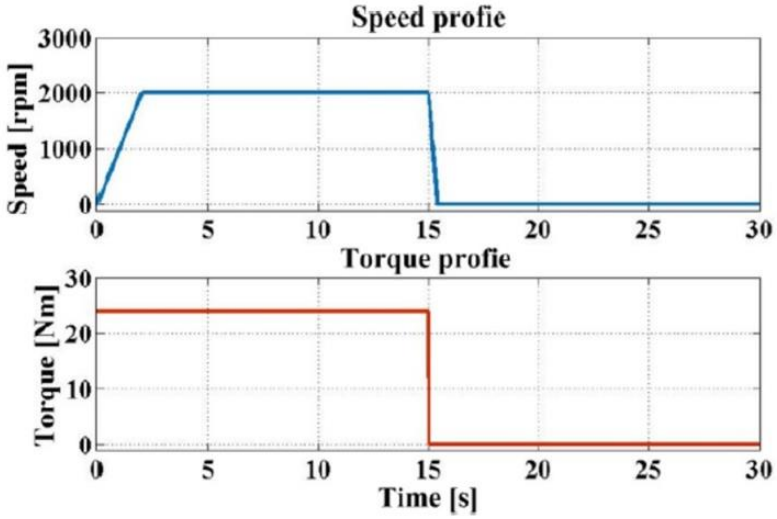


Figure 2.22: Speed-Torque mission profile proposed in [62]

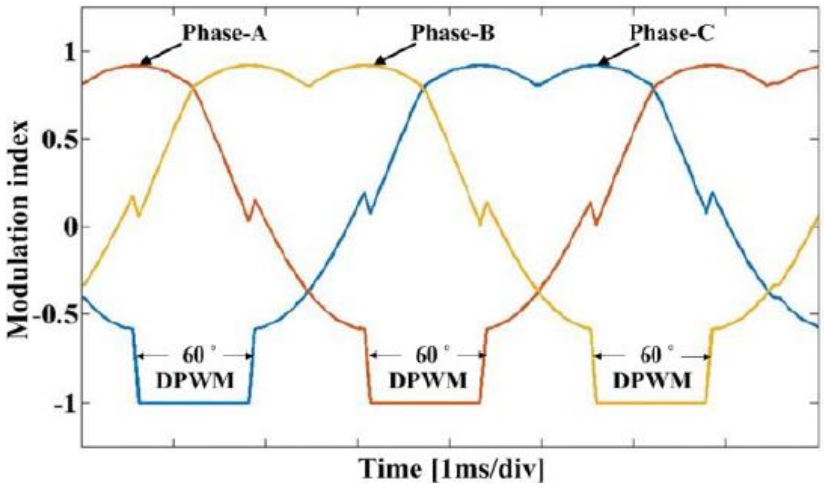
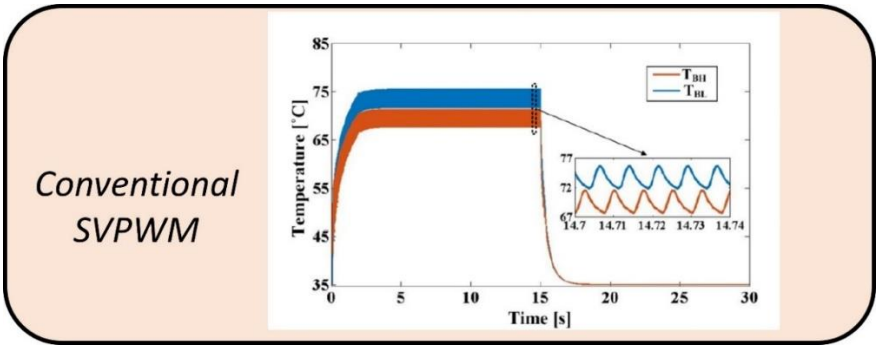
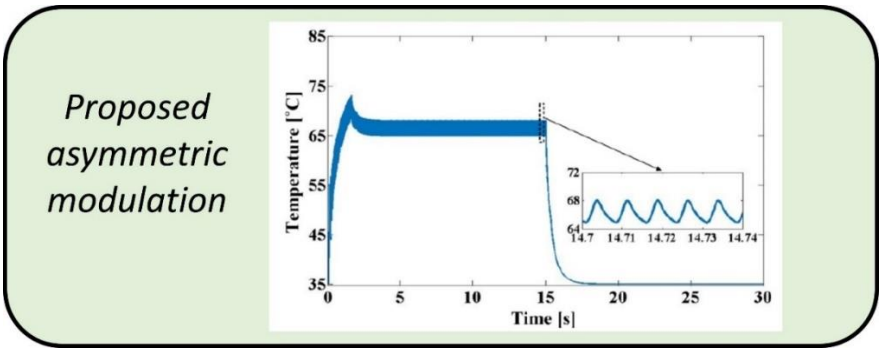


Figure 2.23: Modulation waveform of the proposed asymmetric PWM [62]



(a)



(b)

Figure 2.24: Estimated temperature for (a) conventional SVPWM and (b) proposed asymmetric modulation by [62]

As a brief conclusion, remarks on some of the commonly used modulation techniques for VSIs are given in Table 2.4.

Table 2.4: Remarks on common modulation techniques

Modulation techniques	Observation on the techniques	Remark
DPWM0 [63], [64] DPWM1 [62], [64], [65] DPWM2 [63], [64]	DPWM0, DPWM1, and DPWM2 are three special cases of a Generalized DPWM (GDPWM) method [66]. GDPWM techniques are usually used for losses reduction as they can reduce the losses by up to 50% relative to CPWM methods.	Except for [62], none of the other studies were optimized to improve the reliability of the inverters or power switches' degradation.
DPWM3 [64], [67]	DPWM3 has low harmonic distortion characteristics [67] In [64], the authors concluded that the DPWM3 technique is best applied in AC variable speed drives.	None of the studies comprised the impact of the reliability of the inverters or power switches' degradation
DPWMMAX [63], [64]	The DPWMMAX and DPWMMIN methods have nonuniform thermal stress on the switching devices because of their nonuniformity during the positive and negative halves of the modulating signal cycle. In DPWMMAX, the upper devices have higher conduction losses than the lower ones, while in DPWMMIN, the lower ones have higher conduction losses than the upper ones.	The studies have not directly stated the impact on the lifetime of power switches, but the imbalance between upper and lower switches losses forms a disadvantage in terms of reliability
DPWMMIN [64], [68]		

Table 2.4: Remarks on common modulation techniques (continued)

Modulation techniques	Observation on the techniques	Remark
SPWM [69], [70] SVPWM [69], [70]	In [67], a Permanent Magnet Synchronous Motor PMSM drive was used as an application to compare the two modulation techniques (SPWM and SVPWM) to show their impact on controlling the torque and flux individually. In [68], the comparison was made by applying the two modulation techniques for grid-tie inverters showing the advantage of SVPWM over SPWM, especially in higher power ratings	Both studies focused mainly on the broader voltage utilization range of SVPWM compared to SPWM, but both studies lacked the impact on reliability or thermal stress/cycling for the studied applications
THIPWM [71], [72]	The study [71] showed the advantage of THIPWM over SVPWM in terms of Common Mode Voltage CMV while highlighting the importance and the challenge of synchronizing the injected third harmonic waveform with the modulating signal. An alternating carrier polarity modulation as a modification on conventional THIPWM. In [72], performance improvement in the output voltage THD and DC Bus utilization is present. This improvement was made using an adaptive optimal THIPWM.	The two studies lacked the impact on reliability or thermal stress/cycling for the studied applications

2.5.2 Design of the Converter

Many efforts were made to improve the lifetime of converters by taking some design considerations. For example, in a study regarding electric vehicles' inverters [73], the impact of adopting a variable DC bus voltage and a constant DC bus voltage on the thermal cycling of power switches was studied.

The idea is to use the linear relation between the DC voltage level and the switching losses to reduce the thermal cycling of switches.

$$V_s = 0.5 \times V_{dc} \times m \qquad (2.4)$$

V_s is the stator voltage of the studied PMSM, V_{dc} is the DC Bus voltage, and m is the modulation index.

Briefly, the contribution of their study is to keep the thermal cycling as low as possible by controlling the V_{dc} which directly influences the switching losses and hence the temperature. The required voltage by the motor stator is satisfied by changing the modulation index to satisfy Equation 2.4.

It was found that the use of variable DC bus voltage in [73] improved the lifetime of the inverter by up to 5.06 under specific loading driving cycles. Even if this number might not necessarily be accurate in real applications, but it proves that the consideration of a variable DC bus voltage can be beneficial from a reliability point of view.

In another study [74], the focus is to study the reliability of Modular Multilevel Converters (MMCs) as a solution for the medium voltage stage of smart transformers, which might step in with a managing role in future electrical distribution grid systems. The study investigated the reliability element by studying the impact of transformers'

mission profiles on power semiconductors' thermal stress, which concluded that conditions such as inrush currents and power variations do not have a substantial lifetime reduction effect.

The reliability of multi-MW wind turbines' power converter also received research attention. In the study [75], additional reactive power was introduced to achieve a "smooth thermal control" for multi-MW wind turbine power converters, which basically introduces a reserve of reactive power to flow in the switch in periods where the switch lacks a sufficiently heating power loss. This results in its temperature dropping significantly before heating up again when power loss is resubjected to its junction, leading to high levels of thermal stress. So, the use of reserved reactive power can aid in preventing the switch from cooling down too much by circulating this power through the switches when needed.

Similar to this work in [53], a half-bridge motor drive configuration proposes an active thermal control by reserving some energy in an inductor to use in selected periods. Hence, it prevents the switch from cooling down, decreasing thermal cycling.

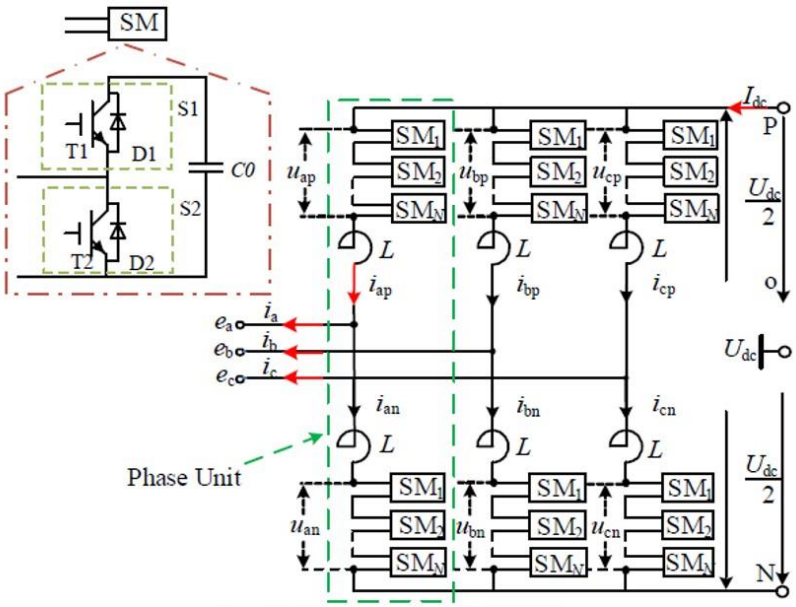
The concept of active thermal control incorporated in the design can be found in literature in two primary forms:

a) Controlling the heat flux from the junction to the ambient by changing the cooling system's performance [1], which will be discussed in further detail in subsection 2.5.3.
b) Controlling the power loss in the semiconductor to influence the junction temperature. as in [2], [4], [61], [76].

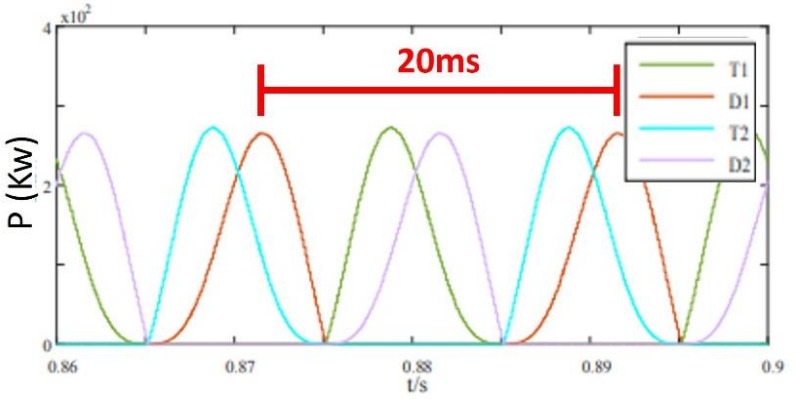
The power loss control is an attractive way of stating that extra loss will be introduced in regions where the power loss is insufficient to keep the junction temperature high enough to maintain the ripple within an acceptable range that ensures a minimum expected lifetime. Hence, less efficiency is imposed.

2.5.3 Active Cooling

Some studies have been made on the controlled system cooling or, as referred to by some authors, "active dynamic cooling". Efforts in [1] and [3] are examples of open-loop and closed-loop control approaches toward active cooling. Although the studies provided some good results, the target application of the methods seems to be aimed toward the very low frequency thermal cycling. Low frequency thermal cycling is an issue for some applications, such as automotive applications, but is not a big issue in most common converters. Concerning other converters applications, the main power cycling challenge is in the order of 50/60 Hz, as it is the frequency of power grids worldwide, or beyond this frequency to the range of 100s Hz or 1000s Hz for industrial motor driving applications. For example, the study [77] clearly shows that the loss waveform for a single switch in an MMC converter featured a period of 0.02s, the same as the time period, as shown in Figure 2.25.



(a)



(b)

Figure 2.25: Modular Multilevel Converter (MMC), (a) basic structure, (b) Conduction power loss distribution per the converter's arm [77]

This power loss waveform would intuitively create thermal cycling fluctuating at a 0.02s frequency. Studies [78], [79] also performed almost the same approach as in [1] and [3] with minor modifications, yet did not contribute to faster thermal cycling problems.

2.6 Lifetime Estimation

IGBTs are widely used in high power applications such as Multi–Mega-Watts wind turbine systems, so the recent lifetime prediction methods for IGBTs will be briefly put in this section.

As covered in Section 2.2, bond wire failures were found to be the most common cause of an IGBT failure, and since the lifetime of a device is the same as the lifetime of its most prone to fail part; then the bond wires failure prediction can be used to estimate the lifetime of the IGBT.

Recent lifetime prediction methods of bond wires can be classified into two categories. The first category depends on empirical lifetime models based on accelerated lifetime testing results, as suggested in [80]–[83]. Empirical-based methods are the most commonly used for IGBT lifetime prediction since they are easier to use because they do not require knowledge of the physical properties of the power semiconductor devices [84]. The second category is based on PoF lifetime models attained from modeling the deformations due to thermal stresses as reviewed in [10]. This approach allows for better comprehension of the mechanisms that lead to bond wire fatigue in IGBTs. However, the drawback of such a method is the lack of ability to include statistical data in such PoF models. Moreover, the limited available information on the materials used, the complexity of the detailed structure that forms the power IGBT, and the manufacturing uncertainties that must be considered to get accurate results. Hence, the use of empirical-based models is considered in most studies.

The empirical approach gained popularity due to its relative feasibility and the complexity of the PoF-based approach. Also, an empirical approach would be convenient when the task is to validate a new design or idea aiming to improve the

system's reliability. Furthermore, several stressing circumstances for different designs can be compared using empirical-based lifetime models without needing a detailed PoF-based model. Although such models might not give a very accurate lifetime prediction, they can prove the potency of an approach.

The optimal approach to study the cycles to failure (N_f) of an IGBT is to use the exact predicted circumstances of the application in which the IGBT will be in placed. However, this approach is impractical due to the very long time required. This is the main reason behind "accelerated testing" emergence; to substantially reduce the testing time.

The Coffin-Manson model is a famous example of the mentioned empirical lifetime models, represented by

$$Nf = A \times (\Delta T_j)^{-\propto} \tag{2.5}$$

Where A and $\propto$ are curve fitting parameters [12]. From the above Equation, the number of cycles to failure (N_f) is inversely proportional to ΔT_j -when $\propto$ is a positive real number-.

Equation 2.5 can be used to compare two similar thermal stress scenarios where they compete in terms of junction temperature fluctuation while the other parameters are the same. Nevertheless, the Equation's effectiveness can be improved by including other driving factors, such as the median temperature T_{jm} (in Kelvin).

$$Nf = A \times (\Delta T_j)^{-\propto} \times e^{\frac{Ea}{K_b \times T_{jm}}} \tag{2.6}$$

Equation 2.6 expresses the lifetime model by the Arrhenius equation [85]. Where Ea is the activation energy, and K_b is the Boltzmann constant. The Norris–Landzberg

model presented in Equation 2.7 goes one step further and includes the cycle frequency (f_c) into the model, while β is a curve fitting parameter [86].

$$Nf = A \times f_c^{\beta} \times (\Delta T_j)^{-\propto} \times e^{\frac{Ea}{K_b \times T_{jm}}} \quad (2.7)$$

Finally, the Bayerer model shown in Equation 2.8 includes the heating time t_{on} effect together with the impact of other bond wire parameters with various curve fitting parameters [81].

$$Nf = A \times (\Delta T_j)^{-\beta_1} \times e^{\frac{\beta_2}{T_{jmin}+273}} \times t_{on}^{\beta_3} \times I^{\beta_4} \times V^{\beta_5} \times D^{\beta_6} \quad (2.8)$$

The values of parameters ($A, \beta_1, \beta_2, \beta_3, \beta_4, \beta_5, \beta_6$) can be taken from the study [81] to reduce the testing time, as they are widely accepted in reliability engineering [18].

2.7 Chapter Summary

This chapter presents an overview of thermal cycling and the degradation and failures it leads to. Failure mechanisms and precursors of failure on the level of power devices were reviewed, emphasizing the effect of temperature fluctuation on the degradation phenomenon of power semiconductors. Moreover, temperature monitoring techniques were discussed, covering the main approaches in the literature to perform junction temperature estimation/measurement for power semiconductor switches. The efforts to determine the effect of modulation techniques and various involved parameters on thermal cycling were also reviewed. Moreover, approaches to mitigate thermal cycling to improve the lifetime expectancy, whether by considering the degradation effect while selecting the modulation technique or by "Active cooling" approaches aiming to decrease ΔT_j are discussed as well.

The chapter is finalized by exhibiting the methods to estimate the lifetime of a power switch using the commonly used lifetime estimation model in literature, such as the physics-of-failure-based method and the more commonly used empirical-based method. The development of empirical models was also addressed in justified steps; to obtain different levels of complexity/accuracy of life estimation and hence, choose the best model for the study.

The contributions in literature towards a more reliable operation took various natures, including modulation parameters optimization. However, this approach is limited since the modulation technique and other operating parameters significantly affect the converter's overall efficiency, cost, and performance. Furthermore, although active cooling methods offered effective ways to improve lifetime expectancy, the studies focused on low frequency thermal cycling. While it is definitely an issue to consider, the contributions did not offer much towards the higher frequency thermal cycling, i.e., thermal cycling at the fundamental frequency of the inverters' output. Therefore, the aforementioned issues are investigated through the development of the double switch H-bridge inverter topology while addressing its positive and negative impact on these issues and its impact on other aspects of the converter in Chapters 3 and 4.

Chapter 3: A Double Switch Single-Phase H-Bridge Inverter for Lifetime Improvement

3.1 Introduction

The inverter's expected lifetime is important for continuous power delivery for different applications. The employment of extra switches in an inverter's topology in such a way that favors reliability by improving the expected lifetime is proposed in this chapter. The principle of operation of the proposed double switch H-bridge is described in detail in Section 3.2. In order to properly evaluate the impact of the proposed method in terms of reliability; Section 3.3 explains the development of the lifetime improvement evaluation curve which purpose is to directly provide the impact on reliability due to any change in the thermal conditions. The followed comparative analysis procedure will be covered in Section 3.4, and a summary of this chapter is drawn in Section 3.5.

3.2 Proposed Double Switch H-Bridge Inverter

This section describes the details of the proposed double switch H-bridge topology for single-phase inverters. The power circuit of the proposed topology and the principle of operation are also explained.

3.2.1 Power Circuit

The proposed topology is a modification of the well-known H-bridge single-phase inverter circuit as shown in Figure 3.1. The labeling of switches shown in Figure 3.1 follows the conventional numbering (S1, S2, S3, and S4), with added labels A and B for each switch as illustrated in Table 3.1. Moreover, to achieve the desired output voltage while achieving a uniform thermal stress distribution, a modified switching

pattern that can accommodate any type of modulation technique is proposed in Section 3.2.2.

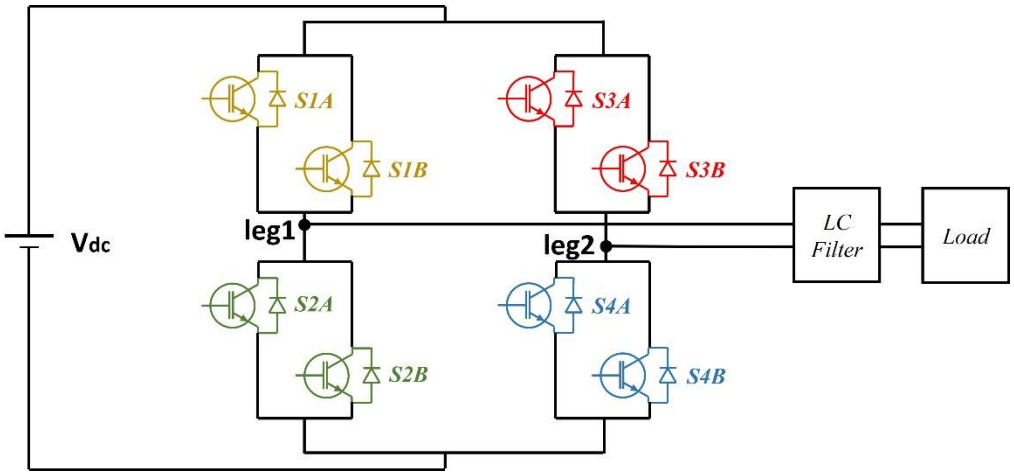


Figure 3.1: Proposed double switch single-phase inverter topology

Table 3.1: Switches labeling approach

Conventional topology	Proposed topology
S1	S1A
	S1B
S2	S2A
	S2B
S3	S3A
	S3B
S4	S4A
	S4B

3.2.2 Modulation Technique and Principle of Operation

In general, the switching operation of a switch under an ordinary switching pattern is split and redistributed on among all eight switches. The resulting switching operation is shown in Figure 3.2 for sinusoidal Unipolar PWM (UPWM).

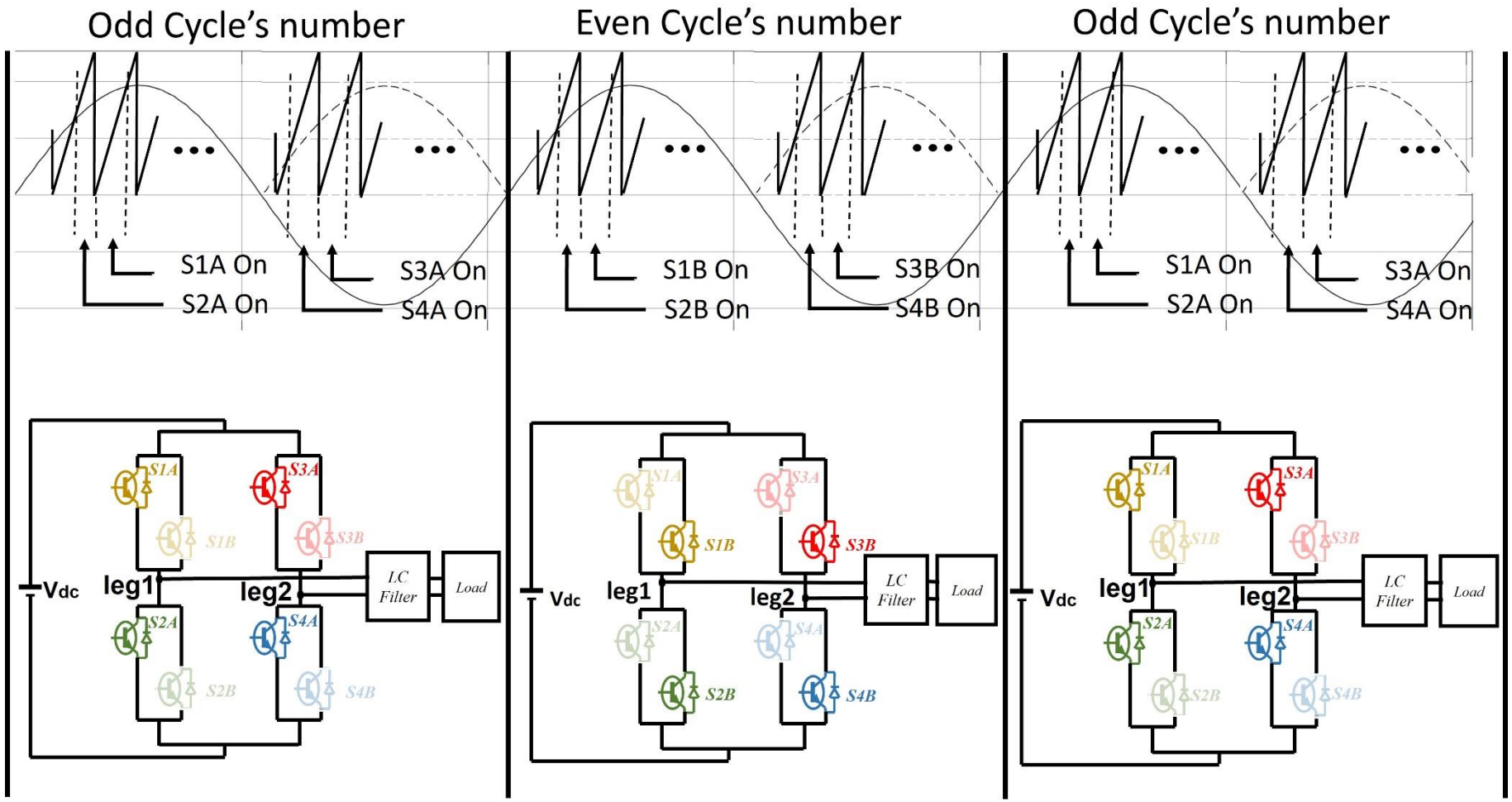


Figure 3.2: Switching operation of UPWM using the proposed topology

As illustrated in Figure 3.2, each switch among the eight switches operates normally for the duration of a single fundamental cycle, then completely rests during the following fundamental cycle's duration as detailed in Figure 3.4.

The output voltage V_o can be expressed in terms of the node voltages V_{leg1} and V_{leg2} as expressed in Equation 3.1. V_{leg1} and V_{leg2} are strictly determined by the switches' states, a mathematical representation is given Equations 3.2 and 3.3.

$$V_o = V_{leg1} - V_{leg2} \tag{3.1}$$

$$V_{leg1} = S_{1A}\, V_{dc} + S_{1B}\, V_{dc}$$
$$\text{Subject to} \tag{3.2}$$

$$S_{1A} \neq S_{1B} \tag{3.3}$$

$$V_{leg2} = S_{3A}\, V_{dc} + S_{3B}\, V_{dc}$$
$$\text{Subject to} \tag{3.4}$$

$$S_{3A} \neq S_{3B} \tag{3.5}$$

Substituting Equations 3.2 and 3.3 into Equation 3.1 yields the output voltage in terms of switches' states as given by Equation 3.6 subject to conditions given in Equations 3.4 and 3.5.

$$V_o = V_{dc}\,[S_{1A} - S_{3A} + S_{1B} - S_{3B}] \tag{3.6}$$

The switching states in the case of UPWM are determined mathematically by comparing a reference signal V_r with a carrier triangular signal V_c, given in Equation 3.7.

$$V_r = m \times sin(2\pi f_f t) \tag{3.7}$$

$$V_c = \frac{2 \times a}{\pi} \times arcsin(sin(\frac{2\pi}{T_s} t)) \quad (3.8)$$

Equation 3.7 describes the reference sinewave signal, where (m) is the modulation index as a value between 0 and 1, (f_f) is the fundamental frequency of the output voltage and it is taken as 50 Hz. Whereas Equation 3.8 describes the carrier triangular wave, where (a) is the amplitude of the triangular frequency taken as 1, (T_s) is the time period for the switching signal (representing the switching frequency of the switches). Figure 3.3 shows the typical signals for Equations 3.7 and 3.8.

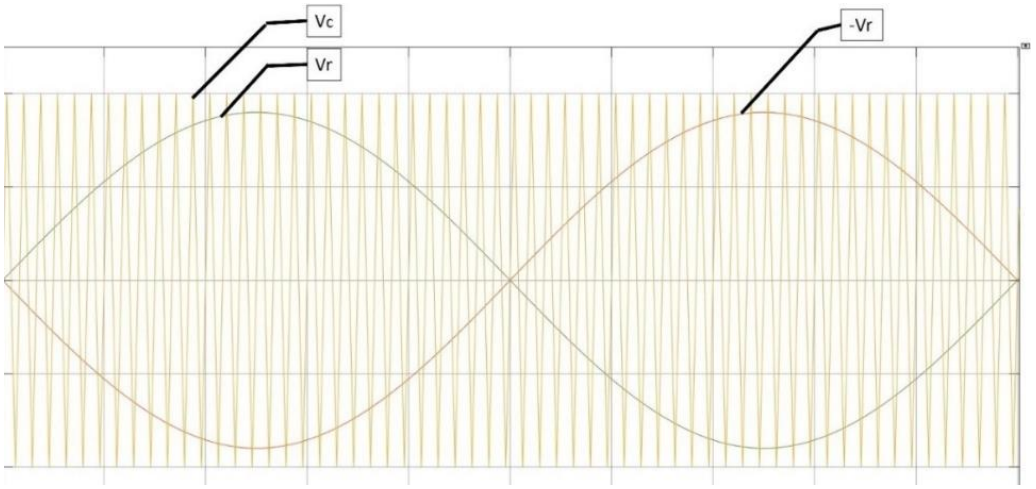


Figure 3.3: Unipolar PWM Reference and carrier signals incorporating 50 Hz reference signal, and 3000 Hz carrier triangular signal

Assuming that switches labeled with A are to be operating at odd fundamental cycles, whereas switches labeled with B are to be operated at even fundamental cycles. Thus, the switching functions for switches labeled with A are given by Equation 3.9.

$$\left.\begin{array}{ll} S_{1A} = \frac{1 + (-1)^{(C_n+1)}}{2} & \\ & , V_r > V_c \\ S_{2A} = 0 & \\ & \\ S_{1A} = 0 & , V_c > V_r \end{array}\right| \quad (3.9)$$

$$\left.\begin{array}{ll} S_{2A} = \dfrac{1+(-1)^{(C_n+1)}}{2} & \\ S_{3A} = \dfrac{1+(-1)^{(C_n+1)}}{2} & , (-V_r) > V_c \\ S_{4A} = 0 & \\ S_{3A} = 0 & \\ S_{4A} = \dfrac{1+(-1)^{(C_n+1)}}{2} & , V_c > (-V_r) \end{array}\right|$$

The switching functions for switches labeled with B are given by Equation 3.10.

$$\left.\begin{array}{ll} S_{1B} = \dfrac{1+(-1)^{(C_n)}}{2} & \\ S_{2B} = 0 & , V_r > V_c \\ S_{1B} = 0 & \\ S_{2B} = \dfrac{1+(-1)^{(C_n)}}{2} & , V_c > V_r \\ S_{3B} = \dfrac{1+(-1)^{(C_n)}}{2} & \\ S_{4B} = 0 & , (-V_r) > V_c \\ S_{3B} = 0 & \\ S_{4B} = \dfrac{1+(-1)^{(C_n)}}{2} & , V_c > (-V_r) \end{array}\right| \quad (3.10)$$

Where C_n is the fundamental cycle's number. This mathematical representation can evenly split the responsibility of the output voltage between the eight switches while achieving the main goal, i.e., decrease the thermal stress on power switches. The switching scenarios are listed in Table 3.2.

Table 3.2: Switching Scenarios and their corresponding unfiltered bridge output

S_{1A}	S_{1B}	S_{2A}	S_{2B}	S_{3A}	S_{3B}	S_{4A}	S_{4B}	V_o
1	0	0	0	0	0	1	0	V_{dc}
0	0	1	0	0	0	1	0	0
1	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	$-V_{dc}$
0	1	0	0	0	0	0	1	V_{dc}
0	0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	$-V_{dc}$

As denoted in Figure 3.4, the switching pattern is split uniformly at every complete fundamental cycle. Intuitively, the proposed inverter's output is identical to the conventional topology's output since no technical intervention on the modulation technique has been done. Switches A and B interchange the responsibility of operating the inverter one cycle at a time. This keeps the operation fixed from the load's point of view while impacting the status of power switches as per Equation 3.6.

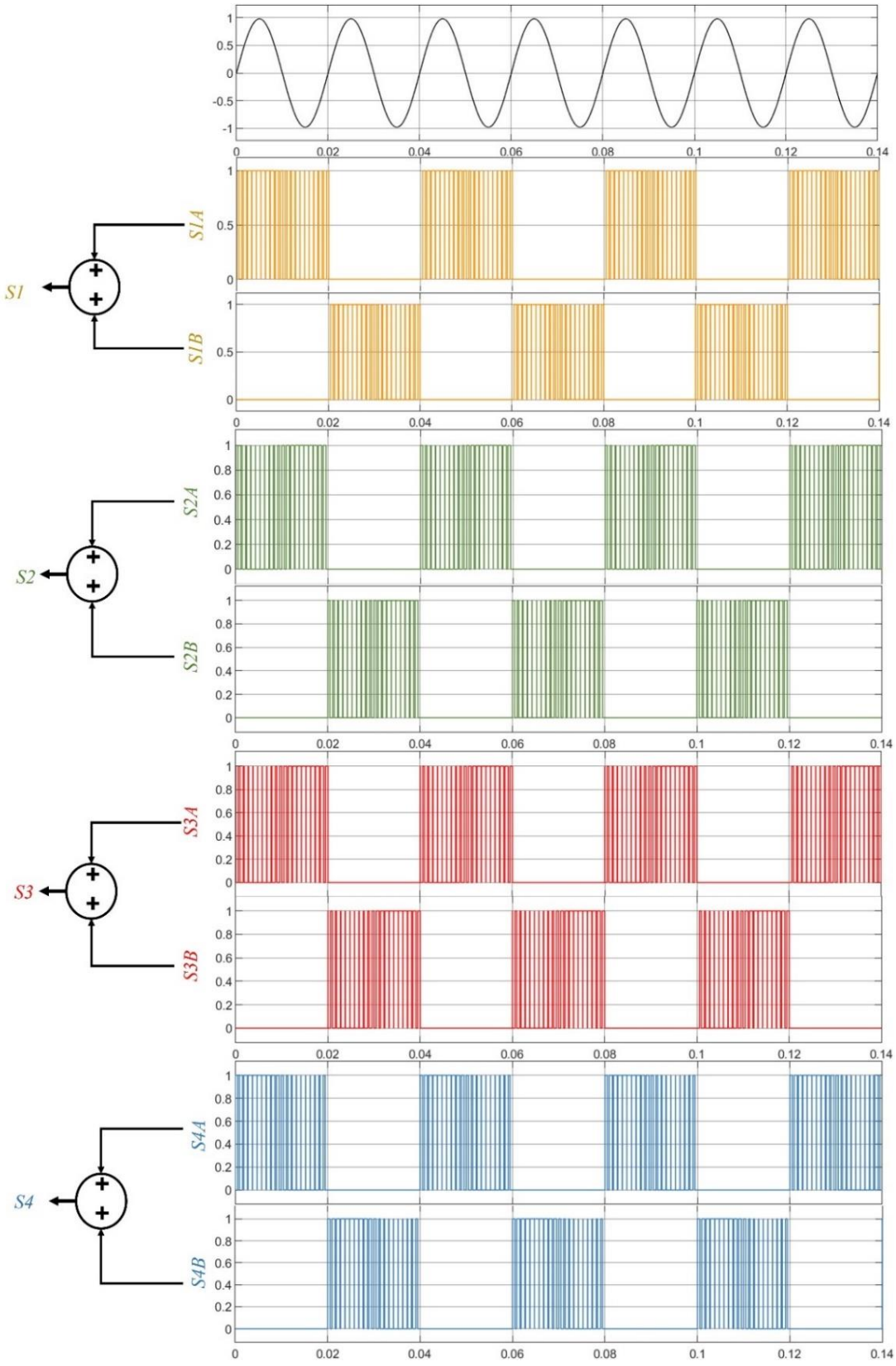


Figure 3.4: Switching pattern for the proposed topology

According to Equations 3.9 and 3.10, the proposed operation logic ensures that at least one backup switch for each main switch (S1-S4) is out of action at all times, as per Figure 3.2. Hence, in case of a destructive transient that leads to a catastrophic failure of power switches in the current path, the inverter can utilize the second switch in a conventional H bridge invert operation mode after the fault is cleared. This backup feature prevents a complete loss of power delivery. However, to utilize this backup feature; an isolation device such as power contactors is needed in series with each switch to isolate any short-circuited or damaged switch from the circuit physically; so the other switch can operate appropriately.

3.3 The Development of the Lifetime Improvement Evaluation Curve

To evaluate the effectiveness and the accuracy of the proposed double switch topology, the performance of this topology must be initially assessed. This performance evaluation approach using the lifetime estimation method is described in Section 3.3.1. Moreover, this section, introduces a novel approach to visualize the lifetime estimating in 2-D lifetime improvement evaluation curves to clearly observe the effect of modifying absolute temperature swing (ΔT_j), and the median temperature of the junction (T_{jm}) on cycles to failure (N_f). Finally, Section 3.3.2 discussed the loading effect on the lifetime improvement of IGBTs.

3.3.1 Lifetime Estimation Model

The lifetime expectancy comparison between the conventional and proposed H-Bridge topologies is made based on IGBTs' estimated lifetime in years. The calculation of IGBTs' lifetime in years can be performed using Equation 3.11, which relies mainly on N_f and the cycling frequency f_c.

$$Lifetime(years) = \frac{N_f}{60 * 60 * 24 * 365 * f_c} \quad (3.11)$$

Here N_f is based on the empirical model given by Equation 2.6. The model shows that N_f for an IGBT directly depends on two factors, namely, ΔT_j, and T_{jm}. Thus, any changes in any of these factors will impact N_f.

According to Equation 2.6, N_f is exponential with respect to ΔT_j at any value of T_{jm}. Moreover, the plot of $\log(N_f)$ vs. $\log(\Delta T_j)$ appears as a straight line, as shown in Figure 3.5 [19].

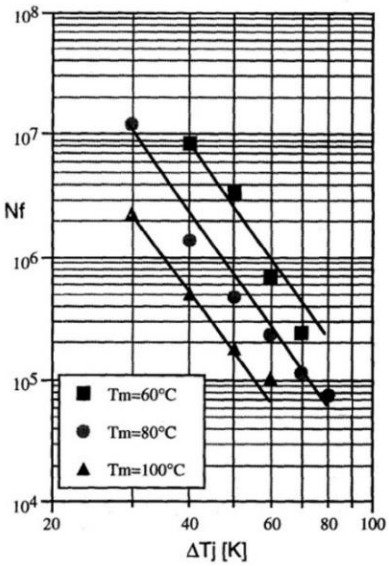


Figure 3.5: Cycles to Failure (N_f) vs. temperature swing in logarithmic means [19]

As seen by Figure 3.5, N_f can be improved significantly by reducing either of ΔT_j or T_{jm}. In order to understand the effect of such reductions in ΔT_j or T_{jm}; new variables can be introduced to the model which are $\%\Delta T_{j\_red}$ (the percentage reduction in ΔT_j), $\%T_{jm\_red}$ (the percentage reduction in T_{jm}), and n (cycles to failure multiplier). Hence, Equation 2.6 can be rewritten such that $\%\Delta T_{j\_red}$ is taken as the subject of the equation

yielding Equation 3.12 which shows the final model after introducing the aforementioned variables.

$$\%\Delta T_{j\_red} = \left(1 - \left[\frac{\left(\frac{n \times N_f}{A \times e^{\frac{E_a}{K_b \times (T_{jm(°C)} \times (1 - \%T_{jm\_red}) + 273.15)}}} \right)^{\frac{-1}{\propto}}}{\Delta T_j} \right] \right) \times 100\% \quad (3.12)$$

After applying the constants as per [87] given in Table 3.3, Equation 3.12 can be rewritten as Equation 3.13.

Table 3.3: The used constants values for the empirical lifetime estimation model as per [91]

Boltzmann-constant (K_b)	9.89×10^{-20}J
Activation energy (E_a)	1.38×10^{-23}J
A	302500
$\propto$	5.039

$$\%\Delta T_{j\_red} = \left(1 - \left[\frac{\left(\frac{n \times N_f}{302500 \times e^{\frac{1.38 \times 10^{-23}}{9.89 \times 10^{-20} \times (T_{jm(°C)} \times (1 - \%T_{jm_{red}}) + 273)}}} \right)^{\frac{-1}{5.039}}}{\Delta T_j} \right] \right) \times 100\% \quad (3.13)$$

Equation 3.13 can help visualize the effect of any change in ΔT_j, and T_{jm}. Solving for $\%\Delta T_{j\_red}$ while taking *n* as 1 and varying $\%T_{jm\_red}$, can yield the required percentage reduction in both ΔT_j, and T_{jm} that keeps N_f constant. Repeating the same procedure for different values of *n* will provide the required percentage reduction in ΔT_j, and T_{jm} to achieve a specific improvement in N_f.

A MATLAB® code was developed to visualize the effect of percentage reduction in T_{jm} and ΔT_j on the estimated N_f by constructing a novel plot satisfying Equation 3.12 for n = (2, 1, 0.5) in one plot. The full code is shown in Figure 3.6.

```
x = [-0.5:0.001:0.5]
DeltaTj= 7;
Tm_c= 75;
Nf= 302500*(DeltaTj)^(-5.039)* exp((9.89e-20)/((1.38e-23)*(Tm_c+273.15)))
y2   = 1-((((Nf*2)./((302500).*exp((9.89e-20)./((1.38e-23).*((Tm_c.*(1-x)+273.15)))))).^(1/-5.039))/(DeltaTj));
y    = 1-((((Nf).*((302500).*exp((9.89e-20).*((1.38e-23).*((Tm_c.*(1-x)+273.15)))))).^(1/-5.039))/(DeltaTj));
y0_5 = 1-((((Nf/2).*((302500).*exp((9.89e-20).*((1.38e-23).*((Tm_c.*(1-x)+273.15)))))).^(1/-5.039))/(DeltaTj));
figure(1)
grid minor
hold on
plot(x*100,y*100,'-','color','k','LineWidth',1,'MarkerFaceColor','g');
ylim([-50,50]);
xticks(-50:5:50);
yticks(-50:5:50);
hold on
set(get(gcf,'CurrentAxes'),'Fontweight','bold','FontName','Arial','FontSize',15);
xlabel('Reduction in Tm(°C) in %','Fontweight','bold','FontName','Arial','FontSize',20);
ylabel('Reduction in ?Tj in %','Fontweight','bold','FontName','Arial','FontSize',20);
plot(x*100,y0_5*100,'-','color','r','LineWidth',1,'MarkerFaceColor','g');
hold on
plot(x*100,y2*100,'-','color','b','LineWidth',1,'MarkerFaceColor','g');
hold on
box on
line([0,0], ylim, 'Color', 'k', 'LineWidth', 0.5); % Draw line for Y axis.
line(xlim, [0,0], 'Color', 'k', 'LineWidth', 0.5); % Draw line for X axis.
```

Figure 3.6: The developed MATLAB code to visualize the effect of percentage reduction in T_{jm} and ΔT_j

The resultant plot shown in Figure 3.7 outlines three main lines (A to C) that separate four regions (1 to 4) on the evaluation curve. Hence, it better shows the impact on N_f when T_{jm} or ΔT_j are reduced. Figure 3.7 incorporates $\%T_{jm\_red}$, and $\%\Delta T_{j\_red}$ as the x and the y axes, respectively. The plot is based on an example when T_{jm} = 75°C, and ΔT_j = 7, where the origin of the plot represents the initial thermal condition (T_{jm} = 75°C, ΔT_j = 7) before any percentage reduction occurs.

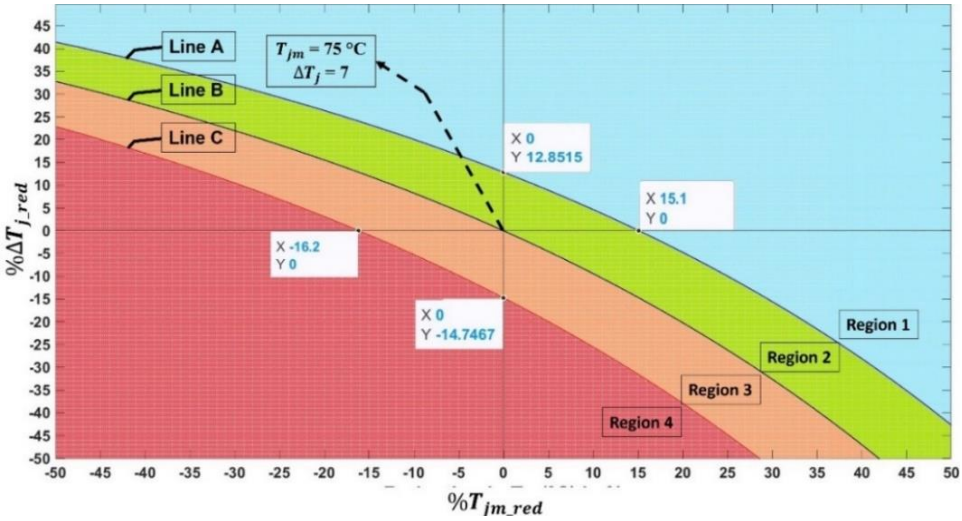


Figure 3.7: IGBTs' novel lifetime improvement evaluation curve, describing the N_f's relationship with the percentage reduction in ΔT_j and T_{jm}

The formation of lines A, B, and C defines the borders of regions 1 to 4. Drifting the operating point from the origin to fall in one of the four regions or on any of the three lines puts N_f into one of the following scenarios described in Table 3.4:

Table 3.4: Impact of thermal condition modification on N_f

Region/Line	Impact on N_f
Region 1	$N_{f-new} > 2\ N_{f-old}$
Line A	$N_{f-new} = 2\ N_{f-old}$
Region 2	$N_{f-old} < N_{f-new} < 2\ N_{f-old}$
Line B	$N_{f-new} = N_{f-old}$
Region 3	$0.5\ N_{f-old} < N_{f-new} < N_{f-old}$
Line C	$N_{f-new} = 0.5\ N_{f-old}$
Region 4	$N_{f-new} < 0.5\ N_{f-old}$

The naming convention of Lines A, B, and C and regions 1 to 4 will be considered for the remainder of the study.

It is worth noting that incorporating the constants listed in Table 3.3 into Equation 2.6 yields the final empirical model for N_f calculation considered for this study, given by Equation 3.14.

$$N_f = 302500 \times (\Delta T_j)^{-5.039} \times e^{\frac{1.38\times10^{-23}}{9.89\times10^{-20}\times T_{jm°K}}} \quad (3.14)$$

3.3.2 The Proposed Method's Expected Impact on Thermal Conditions

As discussed in Section 3.3.1, any change in the thermal condition of IGBT switches will impact the expected lifetime of power switches. This section is to give the effect of adopting the double switch inverter proposed topology on the thermal conditions of IGBTs, namely, T_{jm}, ΔT_j, and f_c. Finally, the Life-Prolonging-Factor (LPF) is introduced and correlated with the initial IGBT thermal loading level before applying the proposed topology.

As covered in Section 3.2, the proposed double switch inverter topology is based on interchangeably feed the inverter's load using eight switches. The principle of operation detailed in Section 3.3.2 shows that the proposed PWM technique drives every IGBT with less on-time relative to the conventional PWM. Hence, reducing the T_{jm} per IGBT. Moreover, the fundamental switching frequency f_c for each switch is reduced to half when compared with the conventional four-switch topology.

Although, the improvement of T_{jm} and f_c comes with the price of putting the switch in a slightly worse situation in terms of ΔT_j. This is simply caused by the break each switch takes for one fundamental cycle after another, which provides more time for

the switch to cool down, leading to increased ΔT_j, the rate at which temperature drops depends on the system's thermal impedance namely, thermal resistance and thermal capacitance, as per the Equation 3.15.

$$T_t = T_i \times e^{-\frac{1}{RC}t} \tag{3.15}$$

Where (T_t) represents the temperature at any instant of the decay period (t), (T_i) represents the initial temperature that the decay starts from (max temperature), and R and C are the thermal resistance and thermal capacitance respectively.

Overall, the lifetime improvement evaluation curve shown in Figure 3.7 can be used to evaluate the effect of replacing the conventional method with the proposed method; since the proposed method impacts , T_{jm}, ΔT_j, and f_c. Doing so will drift the operating point to the right (in the positive direction of $\%T_{jm\_red}$), and down (in the negative direction of$\%\Delta T_{j_red}$), hence, the fourth quadrant of the curve. On the other hand, reducing f_c to half will double the lifetime in years corresponding to any N_f.

3.3.3 Thermal Loading Effect on the Performance of the Proposed Method and its Indices

Evaluation of the reliability of power switches is usually based on N_f. While N_f is commonly accepted as being a measure of reliability, but it is only valid for comparisons where the cycling frequency is the same among the compared scenarios. In this study, a comparison based on N_f is insufficient as the two compared topologies endure thermal cycling at different frequencies f_c. So, the lifetime in years is adopted as one of the indices to compare the two topologies, which can be calculated using Equation 3.11 -assuming a continuous working operation throughout the year for both topologies.

An index is needed to describe the impact of using the proposed method on the expected lifetime for each scenario of loading. A proposed Life-Prolonging Factor (LPF) index is considered for this purpose. LPF is expressed as the ratio of lifetime in years for the proposed method $Lifetime_{(p)}$ to the lifetime in years for the conventional method $Lifetime_{(c)}$, as per Equation 3.16.

$$LPF = \frac{Lifetime_{(p)}}{Lifetime_{(c)}} \tag{3.16}$$

The impact of thermal loading on the LPF takes an exponential nature due to the exponential nature of the lifetime estimation model used in this study. Figure 3.8 shows the nature of the LPF vs. T_{jm_conv} (the junction temperature of the switch at the conventional topology). As per Figure 3.8, the performance/impact of adopting the proposed method increases exponentially with the initial junction temperature when the conventional topology is considered T_{jm_conv}. More detailed loading scenarios will be provided and discussed in Chapter 4.

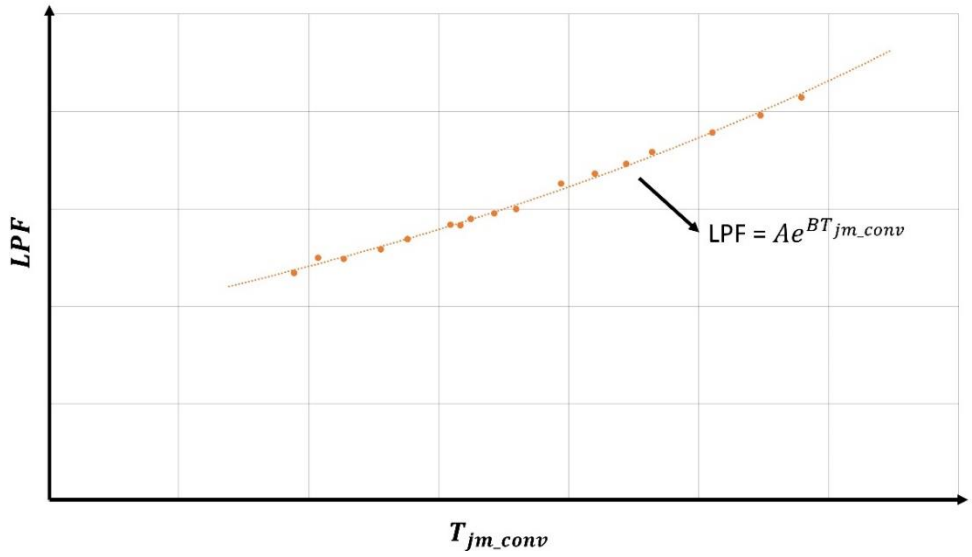


Figure 3.8: Expected exponential behavior of the relationship between LPF vs. T_{jm_conv}

3.4 Tools and Procedure Used for Analysis

3.4.1 PLECS Simulation Software

The main Tool used in this study is PLECS®, which is a software tool specially designed for power electronics simulations. The software includes the possibility to model different physical domains besides the electrical system, such as the thermal domain.

- H-Bridge power circuit design in PLECS

The modeling of an H-Bridge in PLECS is straightforward, the main required components are laid in the workspace, i.e., DC Voltage Source, four power switches (e.g., IGBTs/MOSFETs). Then, the components are connected according to the desired schematic, as shown in Figure 3.9.

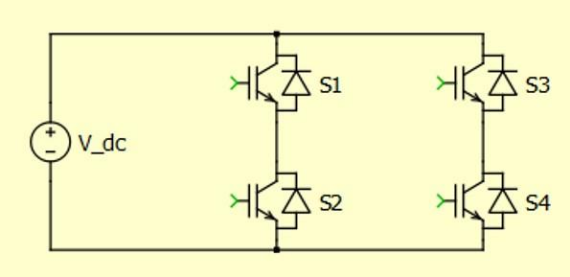


Figure 3.9: PLECS Basic Power Circuit construction

- Thermal components design in PLECS

The thermal domain is a powerful feature of PLECS, which can be done by simply placing the thermal domain components on top of the power circuit such as heatsinks, heat flow meters, constant temperature sources. In the case of an H-bridge, a heatsink component can be placed over the components that are to be simulated with the heatsink. The parameters of the heatsink and the thermal connection between the

components and the heatsink can be done by configuring a thermal network block mediating between the heatsink and the ambient. The Thermal network block represents the thermal impedance between the component's junction and the ambient. Usually, it can be represented by Cauer, or Foster network. Figure 3.10 shows an example of the thermal domain of the H-bridge given in Figure 3.9.

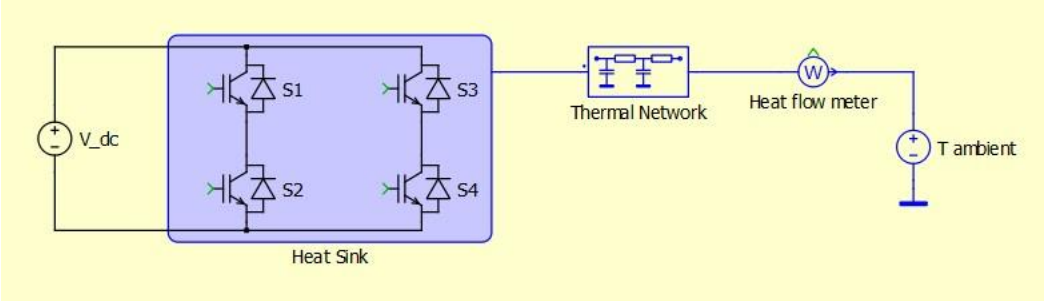


Figure 3.10: PLECS Power Circuit with the thermal domain components

The thermal network block can be configured to as many RC thermal chains as desired, i.e., (thermal resistances and thermal capacitances). The final bit to be configured to obtain thermal related results is the components' thermal descriptions, i.e., switching losses and conduction losses, and internal thermal impedance. which can be done in the losses' configuration window for each power component, as shown in Figure 3.11.

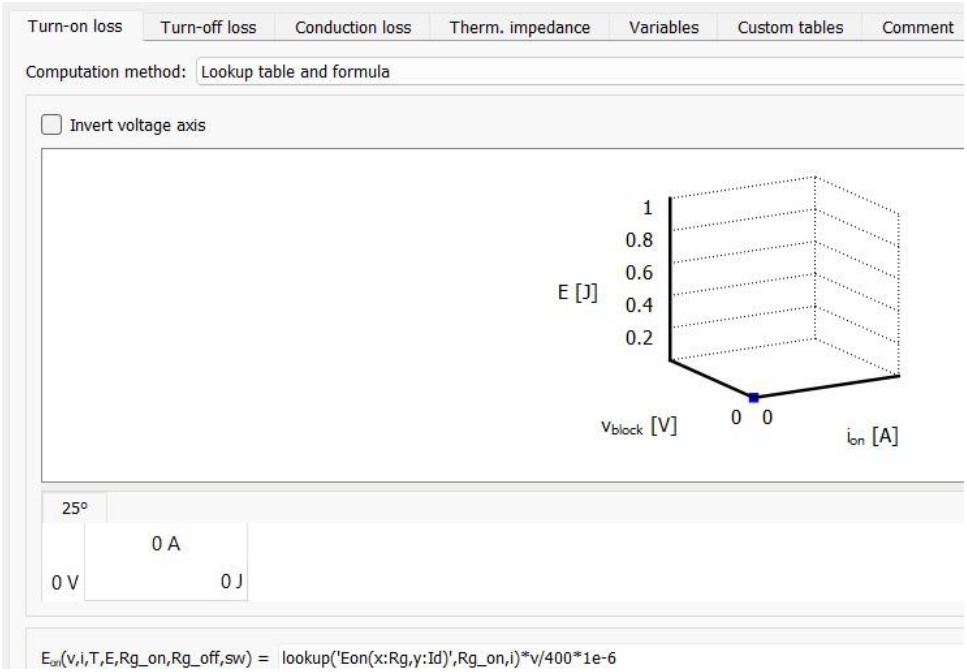


Figure 3.11: Losses configuration window in PLECS

3.4.2 Procedure Adopted for Analysis

This section describes the various tools and methods used in developing the proposed double switch H-bridge topology. In addition, the steps followed to achieve the comparative analysis are detailed.

The two topologies are built and are thermally compared on PLECS® as follows:

Step 1: Implement the desired modulation technique to drive the conventional invert H bridge topology.

Step 2: Apply the split cycle-by-cycle at the fundamental frequency to drive the proposed double switch H bridge topology.

Step 3: Unite all the operational parameters among the two topologies, such as:

- Modulation index.

- Gate resistances.
- Filters.
- Load parameters.
- Thermal descriptions.
- Heatsink and thermal network parameters.

Step 4: Starting with the conventional topology at a specific PF, the load is tweaked until a T_{jm} at the beginning of the studied range is obtained, namely, (~ 40°C).

Step 5: The exact same load is applied to the proposed topology.

Step 6: Extract the instantaneous junction temperature of the power switches T_j, then calculate the absolute temperature swing ΔT_j, and the median temperature of the junction T_{jm}.

Step 7: Calculate the $\%T_{jm\_red}$ and $\%\Delta T_{j\_red}$ and plot the offset of the operating point on the lifetime improvement evaluation curve.

Step 8: Calculate the cycles to failure N_f for each topology.

Step 9: Calculate the estimated lifetime in years and compare the two topologies.

Step 10: Extract the life-prolonging factor LPF for several power levels and power factors.

Steps 4-10 are repeated while tweaking the load to achieve a slightly higher T_{jm} until the full studied range (~ 110°C) is covered with appropriate steps resolution.

The analysis to be carried out in Chapter 4 expected outcomes are as follows:

- To evaluate the relation between the LPF -for different PFs- with the power level (represented by T_{jm_conv} °C).
- To observe the effect of the PF on the LPF at similar power levels.
- To extract approximate trendlines and their equations for each of the studied PFs.
- To extract possible features from the curves of the considered PF values to conclude the overall most beneficial conditions to apply the proposed topology.

3.5 Chapter Summary

This chapter describes the proposed double switch inverter topology as an approach to improve the reliability of IGBTs used in power inverter. The power circuit is provided with the proposed modification that can be applied to any desired modulation technique. The performance evaluation approach is elaborated by discussing the effect of thermal conditions change -regardless of the inducer of that change- on the lifetime. Then it is followed by the performance evaluation procedure in terms of loading conditions, the focus of analysis and its expected outcomes to be carried out in the next chapter.

Chapter 4: Results and Discussion

4.1 Introduction

This chapter provides insights into the test system parameters used to obtain the proposed double switch inverter topology's impact on the power switches' thermal conditions and their expected lifetime. As discussed in Section 3.3.2, the proposed topology will impact the thermal stress that is being subjected to power switches of the inverter in different aspects, namely, median junction temperature T_{jm}, junction temperature swing ΔT_j, thermal cycling frequency f_c and consequently, IGBTs Lifetime. The proposed method's impact on these aspects and the overall performance evaluation process is described in Section 4.3 with some scenarios. Finally, the detailed simulation results of the conventional and the proposed topologies under several identical loading conditions is presented and discussed in Section 4.4.

4.2 Test System Parameters

The principle of operation and the modulation approach for the proposed topology are implemented and evaluated as previously discussed in Chapter 3, as well as the thermal analysis of the system which were carried out in PLECS®. In addition, a manufacturer's official PLECS thermal model for a To-247 single chip (650V/70A Power switch) SCT3030AR from Rohm® is considered [88]; this ensures the best results for the study.

The adopted system for analysis comprised the two topologies simulating the thermal conditions under the exact same electrical conditions in PLECS®. The chosen

electrical and thermal parameters of the testing system for both the conventional topology and the double switch inverter proposed topology are given in Table 4.1.

Table 4.1: PLECS® testing system's parameters

Parameter	**Conventional topology**	**Proposed double switch inverter topology**
DC input voltage	400 V	400 V
AC output voltage	~ 220 VAC	~ 220 VAC
LC Filter	8mH / 4.7uF	8mH / 4.7uF
Load (reflected by T_{jm}°C of the conventional topology)	Variable Load (up to 3KVA at different Power Factors)	Variable Load (up to 3KVA at different Power Factors)
Power switch's Thermal Model	Official SCT3030AR Thermal Model (ROHM) Including the effect of the intrinsic Diode	Official SCT3030AR Thermal Model (ROHM) Including the effect of the intrinsic Diode
Used Thermal Network	R: [0.12, 1.17]* C: [0.3 0.4]*	R: [0.12, 1.17]* C: [0.3 0.4]*
Ambient Temperature	25°C	25°C

*The values for the thermal resistance and thermal capacitance were chosen randomly for comparative purposes. Since both topologies are subjected to the exact same thermal system's parameters, the study can be carried out using an actual extracted thermal network yielding the same conclusions of this study.

4.3 Impact of Adopting the Proposed Topology on IGBT Inverter Lifetime

As discussed in Section 3.3, a lifetime improvement evaluation curve can be produced based on $\%\Delta T_{j\_red}$ and $\%T_{jm\_red}$; to visualize the effect of thermal conditions change on the switches' N_f.

After reproducing the lifetime improvement evaluation curve shown in Figure 3.7 at different thermal conditions, it was found that ΔT_j does not affect lines A, B, and C; hence, it does not affect regions 1 to 4. On the other hand, changing T_{jm} results in a different plot.

In Figure 4.1, a second case where T_{jm} equals 100°C is plotted with the previous case were T_{jm} is 75°C to better observe the effect of T_{jm} on the nature of the plot.

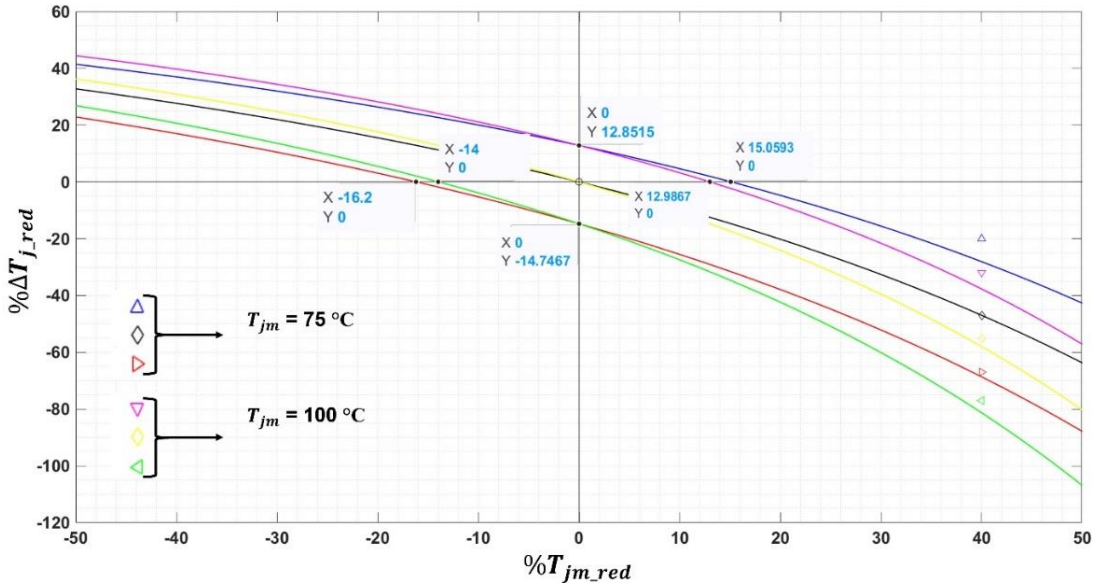


Figure 4.1: IGBTs' lifetime improvement evaluation novel curve, comparing two median temperatures of 75°C and 100°C

It can be denoted from Figure 4.1 that higher median junction temperatures give more chance to improve the expected N_f. For example, region 1 (which indicates a significant improvement in lifetime) in the case of 100°C, $\%T_{jm\_red}$ has a closer boundary to the origin, where the zero crossing of line A is at 12.99%. On the other hand, line A is at 15.06% in the case of 75°C T_{jm}. Hence, it is easier to improve the expected lifetime of IGBTs operating under higher T_{jm}.

In the proposed topology, each of the four switches in a single-phase full-bridge is replaced by a pair of switches in parallel; the main intent is to split the thermal cycles among them. Hence, the rate at which thermal cycling (f_c) occurs is reduced to half compared to the conventional topology built with four switches.

Figure 4.2 shows the effect on the switches' instantaneous temperature waveforms when adopting the proposed double switch topology in contrast with the conventional topology.

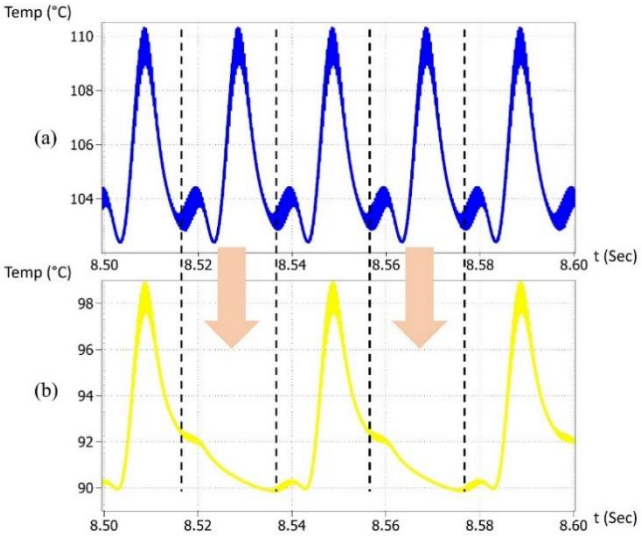
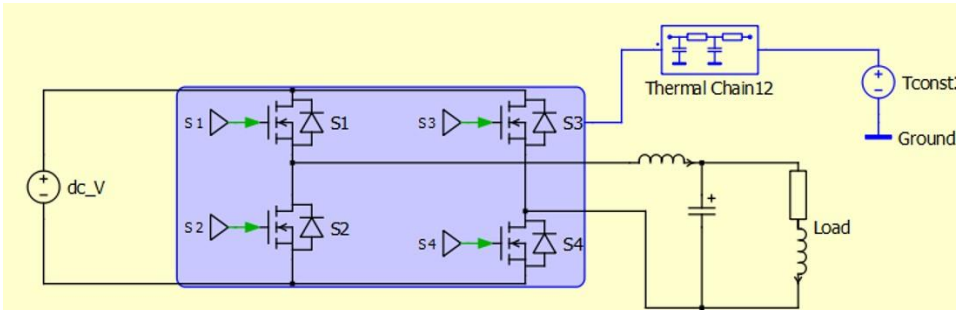


Figure 4.2: IGBT's junction temperature for (a) conventional topology and (b) proposed topology

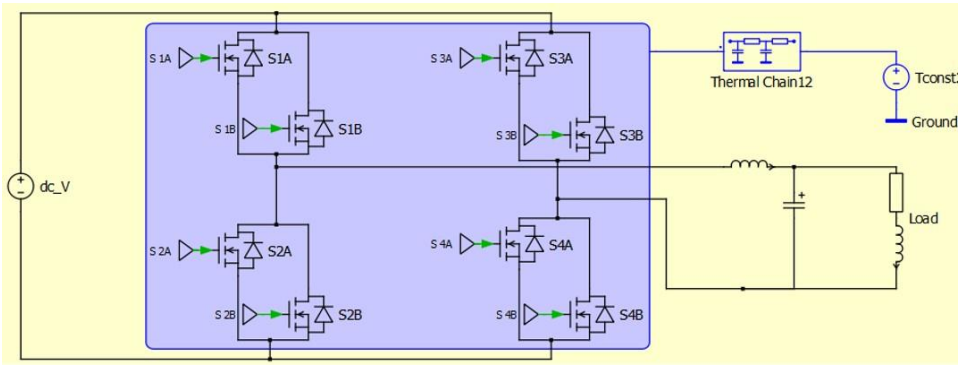
Both topologies are feeding the same arbitrary load and are operating under the exact same circumstances. As a result, T_{jm} is reduced indefinitely since the losses per switch are reduced. More importantly, the cycling frequency f_c is effectively reduced to half to be 25 Hz for the proposed topology compared to 50 Hz in the case of the conventional topology.

As discussed previously in Section 3.3.2, the impact of adopting the proposed method has a positive impact (the reduction of T_{jm} and f_c) and a negative impact (the increase in ΔT_j). Nevertheless, the overall impact was found to be beneficial. To prove this claim, multiple operating points are simulated in PLECS® for both topologies (a) and (b), shown in Figure 4.3.

The impact on T_{jm} and ΔT_j is evaluated by following the novel approach explained in Section 3.3, namely, the lifetime improvement evaluation curve. The chosen electrical loading levels are represented by thermal means i.e., (T_{jm_conv}). The power factor is kept constant for all the scenarios for both topologies. The sample scenarios and their results are listed in Table 4.2.



(a)



(b)

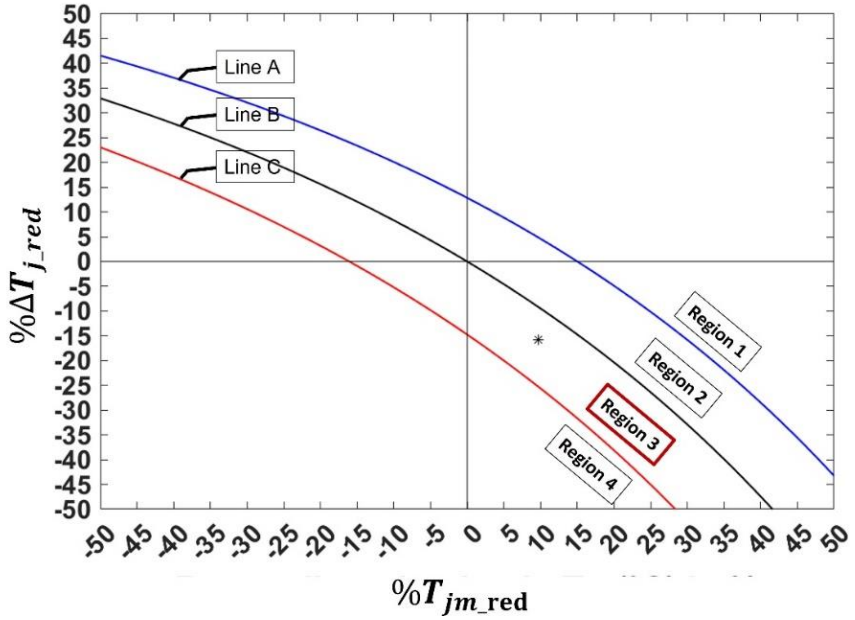
Figure 4.3: The compared two topologies on PLECS (a) conventional topology, (b) proposed topology

Table 4.2: Results of adopting the proposed topology at several loading scenarios

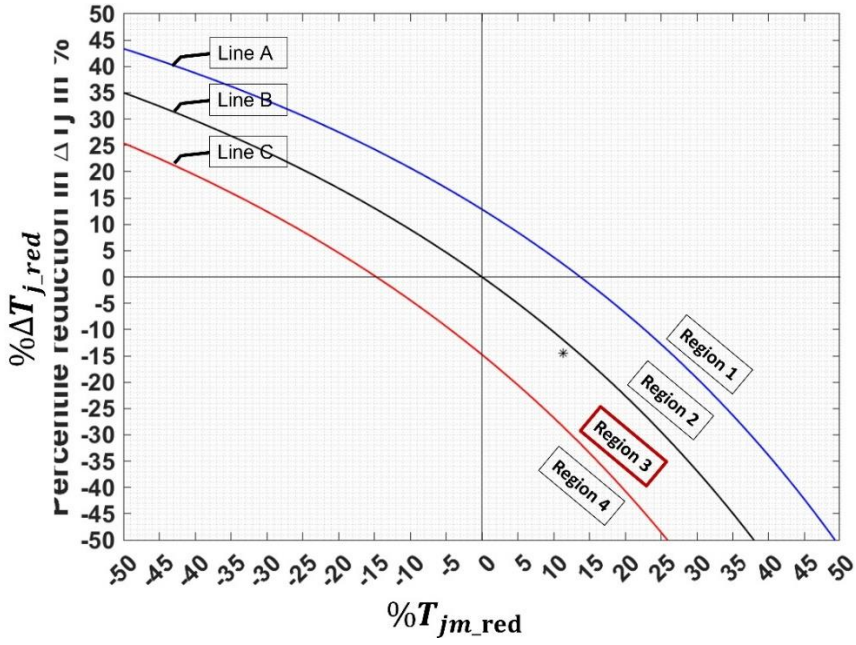
Scenario	**Conventional topology's T_{jm} and ΔT_j**	**Proposed topology's T_{jm} and ΔT_j**	**$\%T_{jm\_red}$ and $\%\Delta T_{j\_red}$**
Scenario 1	T_{jm} = 75.9°C	T_{jm} = 68.55°C	9.68%
	ΔT_j = 5.18	ΔT_j = 6.00	-15.83%
Scenario 2	T_{jm} = 89.56°C	T_{jm} = 79.43°C	11.31%
	ΔT_j = 6.55	ΔT_j = 7.5	-14.5%
Scenario 3	T_{jm} = 96.72°C	T_{jm} = 85.23°C	11.88%
	ΔT_j = 7.27	ΔT_j = 8.3	-14.17%
Scenario 4	T_{jm} = 104.07°C	T_{jm} = 91.14°C	12.42%
	ΔT_j = 7.99	ΔT_j = 9.12	-14.14%

As clearly denoted in Table 4.2, T_{jm} is reduced in all scenarios ranging from a 9.68% reduction up to a 12.42% reduction, which has a positive impact on the lifetime. On the other hand, ΔT_j is increased for all the scenarios, which forms a negative impact on the lifetime. Hence, the operating point drifts to the fourth quadrant of the lifetime improvement evaluation curve. An individual lifetime improvement evaluation graph is produced for each scenario; to classify into which region the operating point drifts to (when shifting from the conventional topology to the proposed topology). In this way, a better understanding of the effectiveness of the proposed double switch inverter topology under specific loading conditions can be gained.

As shown in Figure 4.4, in scenarios 1, 2, and 3, the operating point moved into region 3, while in scenario 4, the operating point entered region 2, as per the previously defined regions in Figure 3.7.

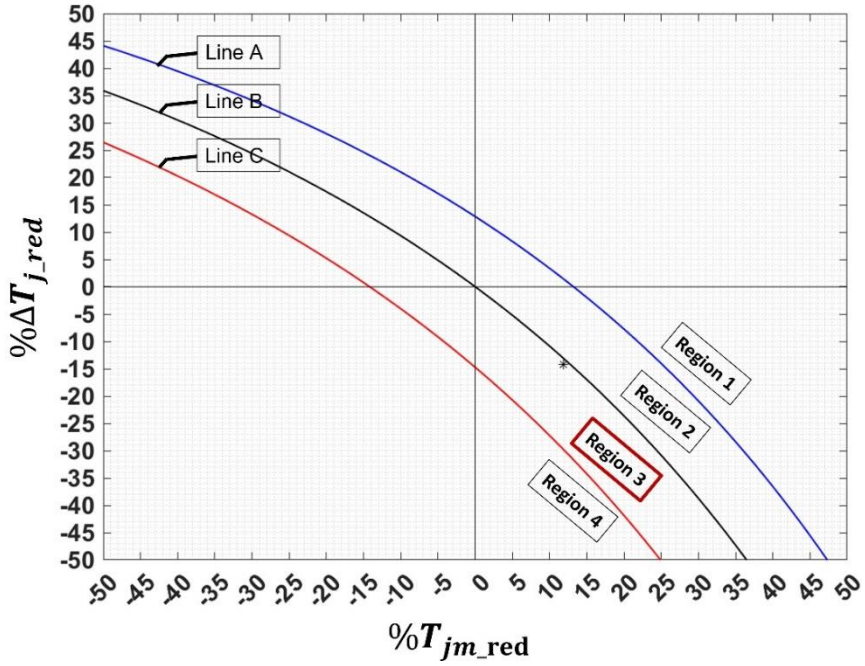


(a)

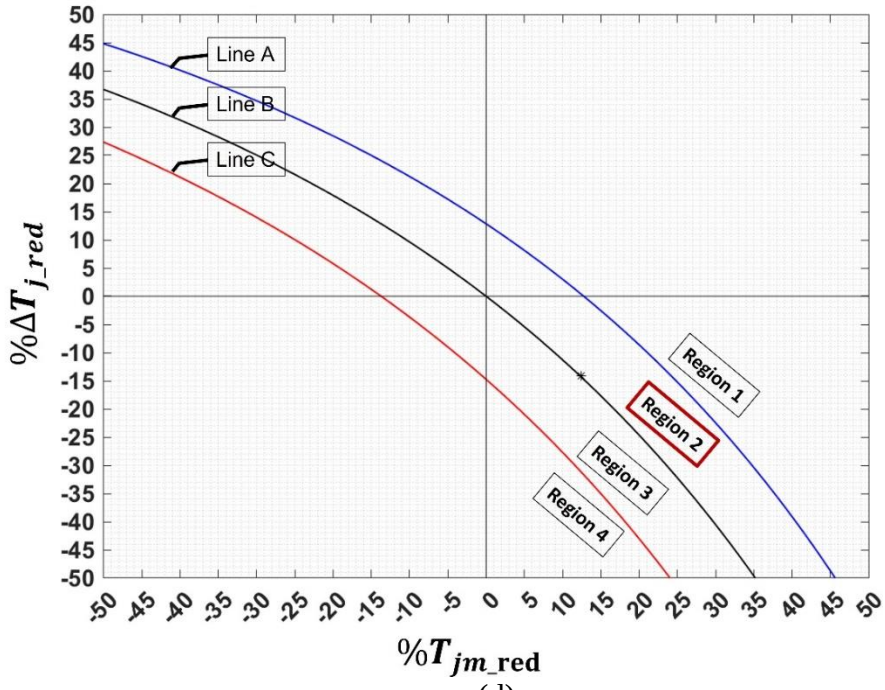


(b)

Figure 4.4: Results for adopting the proposed topology for [(a) scenario 1, (b) scenario 2, (c) scenario 3, and (d) scenario 4] as per Table 4.2



(c)



(d)

Figure 4.4: Results for adopting the proposed topology for [(a) scenario 1, (b) scenario 2, (c) scenario 3, and (d) scenario 4] as per Table 4.2 (continued)

Normally, drifting the operating point into region 3 with f_c constant is harmful since it would decrease the estimated lifetime to the range of [(0.5 – 1) times of the original value]. However, offsetting the operating point as a result of using the proposed topology comes with the significant advantage of reducing f_c to half; hence, achieving double the lifetime for the same N_f compared to the conventional method. So, the impact on lifetime for scenarios 1, 2, and 3 will boost the lifetime to fall in the range of [(1 – 2) times of the original value]. Similarly, in scenario 4, a lifetime boost will be in the range of (2 – 4) times of the original value. Overall, the detailed impact on lifetime when adopting the proposed topology in the previous scenarios is given in Table 4.3.

Table 4.3: Proposed topology's impact on the estimated lifetime in years

Operating point offsetting to:	**Impact on the estimated lifetime**
Region 1	Lifetime(years)-new > 4 Lifetime(years)-old
Line A	Lifetime(years)-new = 4 Lifetime(years)-old
Region 2	2 Lifetime(years)-old < Lifetime(years)-new < 4 Lifetime(years)-old
Line B	Lifetime(years)-new = 2 Lifetime(years)-old
Region 3	Lifetime(years)-old < Lifetime(years)-new < 2 Lifetime(years)-old
Line C	Lifetime(years)-new = Lifetime(years)-old
Region 4	Lifetime(years)-new < Lifetime(years)-old

As per Table 4.3, adopting the proposed topology may lead to offset the operating point from the origin of the graph into any region or fall on top of any line. All of which are beneficial except for line C and region 4. Where line C indicates no gains on the lifetime, while region 4 implies a decrease in the estimated lifetime. Concerning the five remaining scenarios, they all guarantee a life-prolonging factor LPF > 1 as per Equation 3.16.

4.4 Results of the Conventional and the Proposed Topologies with Several Identical Loading Conditions

This section presents the test results of the proposed double switch H-Bridge topology in contrast with the conventional method, while focusing on T_{jm} and ΔT_j imposed on IGBTs by the two topologies. The following scenarios are considered in the simulation:

I. Three values of PF are considered as Low, Medium, and High. Namely, 0.6, 0.78, 0.97.

II. Considering each of the three PFs mentioned, various loading conditions were applied identically to both topologies such that the T_{jm_conv} spans from ~40°C to ~110°C.

III. The LPF for each PF case is scattered on an LPF vs T_{jm_conv}; to find an exponential equation describing the behavior of LPF for each of three PFs.

Table 4.4 provides the detailed results of the two topologies for a PF of 0.6 with various loading levels. While Table 4.5 and Table 4.6 show the corresponding results for a PF of 0.78 and a PF of 0.97, respectively. These experiments cover an adequate range of power factors at various power levels. Hence, this can help comprehensively understand the impact of applying the proposed topology under any loading condition.

Table 4.4: Detailed comparison results between the conventional and the proposed topologies for the case of a PF = 0.6

Topology	T_{jm}°C	ΔT_j	N_f	Lifetime (years)	$\%T_{jm\_red}$°C	$\%\Delta T_{j\_red}$	LPF
Conventional	39.1	1.32	6.93342E+14	439714.799	5.677749361	-19.6969697	0.953
New	36.88	1.58	3.30265E+14	418904.878			
Conventional	40.04	1.42	4.47942E+14	284082.895	5.844155844	-19.71830986	0.959
New	37.7	1.7	2.14872E+14	272542.198			
Conventional	41.6	1.56	2.48996E+14	157912.299	6.274038462	-19.87179487	0.971
New	38.99	1.87	1.20843E+14	153276.64			
Conventional	46.99	2.06	4.18102E+13	26515.831	7.490955522	-19.90291262	1.028
New	43.47	2.47	2.14854E+13	27251.934			
Conventional	48.56	2.21	2.63039E+13	16681.835	7.804777595	-19.90950226	1.045
New	44.77	2.65	1.37408E+13	17428.691			
Conventional	51.26	2.46	1.27342E+13	8075.957	8.310573547	-19.91869919	1.074
New	47	2.95	6.84104E+12	8677.115			
Conventional	54.48	2.76	5.7393E+12	3639.838	8.847283407	-19.92753623	1.11
New	49.66	3.31	3.18444E+12	4039.113			
Conventional	58.35	3.12	2.39691E+12	1520.108	9.42587832	-19.87179487	1.156
New	52.85	3.74	1.38484E+12	1756.517			
Conventional	62.92	3.55	9.32011E+11	591.077	9.837889383	-20.28169014	1.177
New	56.73	4.27	5.48376E+11	695.555			
Conventional	69.98	4.24	2.45568E+11	155.738	10.83166619	-18.63207547	1.355
New	62.4	5.03	1.66407E+11	211.07			
Conventional	79.64	5.09	55200640706	35.008	12.33048719	-18.4675835	1.523
New	69.82	6.03	42041703939	53.325			
Conventional	91.34	6.16	10995193379	6.973	13.76176921	-17.85714286	1.764
New	78.77	7.26	9697184029	12.3			
Conventional	101.53	7.09	3171448666	2.011	14.66561607	-17.63046544	1.948
New	86.64	8.34	3088112343	3.917			

For the case of 0.6 PF given in Table 4.4, in the lower load range (i.e., T_{jm_conv} < ~ 47°C), the value of LPF fall in the range of (LPF < 1) , which is a drift of the operating point into ‘region 4’ according to the lifetime improvement evaluation curve’s regions given in Table 4.3. Hence, this operating range is not beneficial to apply the double switch H-bridge proposed topology; since it will decrease the expected lifetime rather than improving it as intended. Whereas, for higher loads such that the T_{jm_conv} > ~ 47°C, the LPF surpassed the value of 1 and fell in the range of (1 < LPF < 2), which is a drift of the operating point into ‘region 3’ according to the lifetime improvement evaluation curve. indicating an improvement in the expected lifetime. For this case, it is clear that the higher the load gets, the better LPF gets. Hence, the most beneficial condition to apply the proposed double switch H-bridge topology at low power factors is when the switches are already highly thermally loaded in the conventional topology.

Table 4.5: Detailed comparison results between the conventional and the proposed topologies for the case of a PF = 0.78

Topology	T_{jm}°C	ΔT_j	N_f	Lifetime (years)	$\%T_{jm\_red}$°C	$\%\Delta T_{j\_red}$	LPF
Conventional	41.43	1.7	1.63478E+14	103677.027	5.044653633	-15.29411765	1.137
New	39.34	1.96	9.29364E+13	117879.765			
Conventional	45.73	2.13	3.85984E+13	24478.945	5.882352941	-15.96244131	1.148
New	43.04	2.47	2.21571E+13	28103.853			
Conventional	50.21	2.59	1.05543E+13	6693.484	6.61222864	-16.21621622	1.18
New	46.89	3.01	6.22874E+12	7900.478			
Conventional	55.47	3.13	2.85057E+12	1807.822	7.355327204	-15.97444089	1.247
New	51.39	3.63	1.77697E+12	2253.893			
Conventional	60.76	3.66	9.17381E+11	581.799	7.982225148	-16.12021858	1.292
New	55.91	4.25	5.9274E+11	751.826			
Conventional	65.35	4.12	3.77633E+11	239.493	8.462127008	-16.26213592	1.33
New	59.82	4.79	2.51209E+11	318.631			
Conventional	71.82	4.77	1.21348E+11	76.958	9.078251184	-16.14255765	1.404
New	65.3	5.54	85182390500	108.045			
Conventional	75.9	5.18	62822796815	39.842	9.683794466	-15.83011583	1.483
New	68.55	6	46593372447	59.099			
Conventional	79.47	5.55	36045909972	22.86	10.28060903	-14.77477477	1.617
New	71.3	6.37	29150644510	36.974			
Conventional	84.9	6.09	16588297936	10.52	10.90694935	-14.61412151	1.711
New	75.64	6.98	14193333702	18.003			
Conventional	89.56	6.55	8887225209	5.636	11.31085306	-14.50381679	1.783
New	79.43	7.5	7923480706	10.05			
Conventional	96.72	7.27	3584431850	2.273	11.87965261	-14.16781293	1.909
New	85.23	8.3	3421759418	4.34			
Conventional	104.07	7.99	1526849784	0.968	12.42432978	-14.14267835	2.017
New	91.14	9.12	1538771767	1.952			

For the case of 0.78 PF given in Table 4.5, in contrast with the lower PF results in Table 4.4, the mid-range PF featured a value of LPF in the range of (1 < LPF < 2) for the same relatively lower loading range (i.e., T_{jm_conv} < ~ 47°C). Which is a drift of the operating point into ‘region 3’ according to the lifetime improvement evaluation curve’s regions given in Table 4.3. Moreover, similar to the lower PF value, the more the switches are thermally loaded, the more beneficial the proposed topology would be. As T_{jm_conv} slightly surpassed ~104°C, The operating point in the lifetime improvement evaluation curve entered ‘region 2’ indicating an LPF in the range of (2 < LPF < 4).

Table 4.6: Detailed comparison results between the conventional and the proposed topologies for the case of a PF = 0.97

Topology	T_{jm}°C	ΔT_j	N_f	Lifetime (years)	$\%T_{jm\_red}$°C	$\%\Delta T_{j\_red}$	LPF
Conventional	37.77	1.44	4.93366E+14	312890.975	3.177124702	-13.19444444	1.171
New	36.57	1.63	2.88888E+14	366423.557			
Conventional	45.41	2.31	2.62324E+13	16636.479	4.360273068	-12.98701299	1.244
New	43.43	2.61	1.63205E+13	20700.833			
Conventional	51.09	2.94	5.24712E+12	3327.699	5.0499119	-12.92517007	1.294
New	48.51	3.32	3.39549E+12	4306.808			
Conventional	55.2	3.41	1.8846E+12	1195.205	5.452898551	-12.60997067	1.345
New	52.19	3.84	1.26772E+12	1607.961			
Conventional	61.81	4.16	4.49884E+11	285.315	6.002265006	-12.25961538	1.419
New	58.1	4.67	3.19223E+11	404.9			
Conventional	64.96	4.51	2.45328E+11	155.586	6.25	-12.19512195	1.449
New	60.9	5.06	1.7775E+11	225.457			
Conventional	71.94	5.28	72209842309	45.795	6.769530164	-12.31060606	1.5
New	67.07	5.93	54153895895	68.688			
Conventional	78.81	6.05	24245704159	15.377	7.63862454	-11.73553719	1.63
New	72.79	6.76	19755427717	25.058			
Conventional	84.04	6.62	11431793380	7.25	8.055687768	-11.78247734	1.681
New	77.27	7.4	9609589407	12.189			
Conventional	92.82	7.6	3523283277	2.234	8.597285068	-11.44736842	1.793
New	84.84	8.47	3157481308	4.005			
Conventional	102.1	8.62	1150866154	0.73	9.138099902	-11.36890951	1.89
New	92.77	9.6	1088590653	1.381			
Conventional	109.49	9.43	506164521.4	0.321	9.562517125	-11.2407211	1.981
New	99.02	10.49	501187560.9	0.636			
Conventional	115.78	10.13	260639526.2	0.165	9.8894455	-10.95755183	2.073
New	104.33	11.24	269919946.3	0.342			

Finally, for the case of the highest considered PF in this study with the value of 0.97 given in Table 4.6. In comparison with the previously discussed PF values, this case showed even better results in the lower loading range, where it featured a value of LPF in the range of (1 < LPF < 2) for even lower loading conditions (i.e., T_{jm_conv} = ~ 38°C), Which is a drift of the operating point into 'region 3' according to the lifetime improvement evaluation curve's regions given in Table 4.3, in contrast with the case of 0.6 PF where the LPF didn't exceed the value of 1 for T_{jm_conv} < ~ 47°C. On the other hand, the LPF didn't surpass the value of 2 even for a T_{jm_conv} > 109°C, in contrast with the case of 0.79 PF where the LPF exceeded the value of 2 for a loading condition as low as T_{jm_conv} = ~ 104°C.

It is noteworthy that at very low temperatures, the expected lifetime shows a number in the range of tens of thousands to hundreds of thousands of years, this indicates that the power switch is very unlikely to fail due to thermal cycling but rather will fail due to other factors, such as high surges of voltage or short circuit current, metallization, or mechanical damage.

The results indicate a varying behavior for the different PF values at different loading conditions, where no PF value showed superiority over the others in all loading conditions. Therefore, more analysis per loading range comparing the three PFs is required to better understand their effect on the performance of the proposed topology.

The results from Table 4.4, Table 4.5, and Table 4.6 are scattered as shown in Figure 4.5. This shows the relation between the LPF and the (T_{jm_conv}°C), Moreover, three exponential trendlines to approximate the LPF at the three studied PFs were extracted and are documented in Table 4.7.

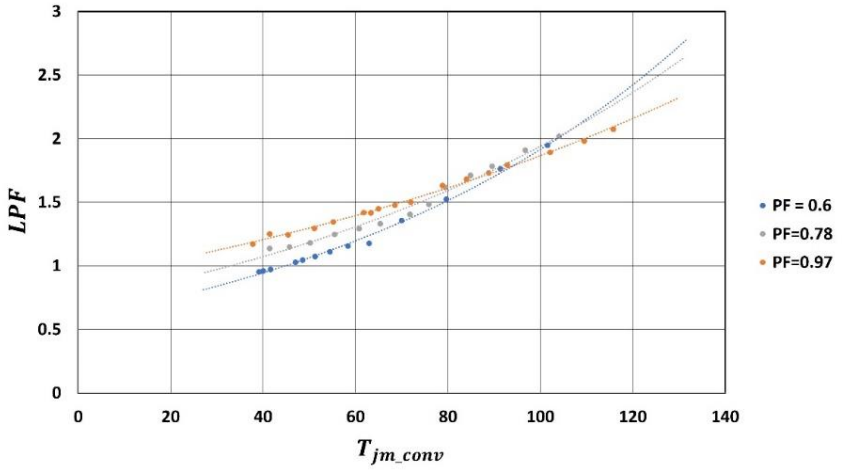


Figure 4.5: Effect of (T_{jm_conv}°C) for each studied power factor on the LPF

Table 4.7: Approximated trendlines' equations for LPF with respect to of T_{jm_conv}°C for each studied power factor value

Power factor	Approximate trendlines' equation
0.6	$LPF_{(PF=0.60)} = 0.5904e^{0.0118\ T_{jm\_conv}{}^{\circ}C}$
0.78	$LPF_{(PF=0.78)} = 0.7225e^{0.0099\ T_{jm\_conv}{}^{\circ}C}$
0.97	$LPF_{(PF=0.97)} = 0.9014e^{0.0073\ T_{jm\_conv}{}^{\circ}C}$

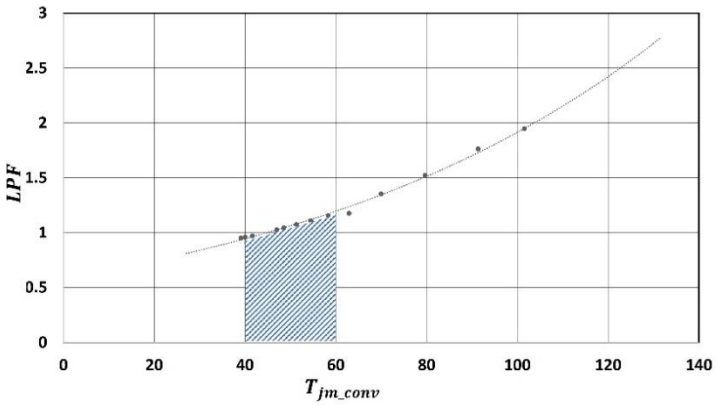
To evaluate the effectiveness of the proposed method under different loading conditions, a feature can be extracted from the curves' equations in Table 4.7.

The average value of LPF within a specific range of T_{jm_conv}°C can be a helpful feature. The higher the average value within a specific range, the better the performance of the proposed topology in that range. Hence, the trendlines for the different power factors can be integrated over specific periods of T_{jm_conv}. The loading ranges can be divided as expressed in Table 4.8.

Table 4.8: Selected loading ranges in terms of T_{jm_conv}°C

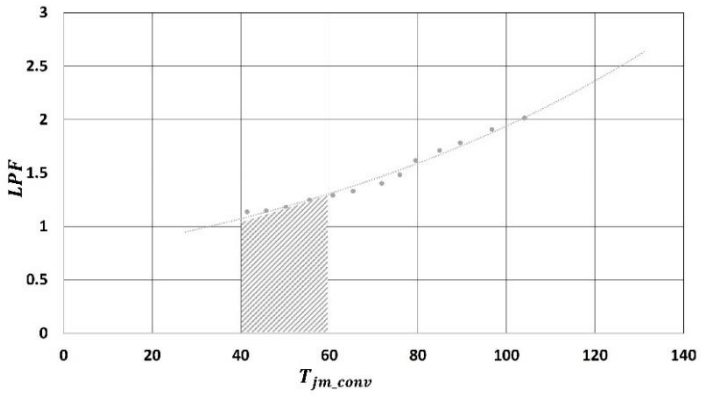
Selected loading ranges for analysis
$T_{jm\_conv} \in [40,60]$°C
$T_{jm\_conv} \in [60,80]$°C
$T_{jm\_conv} \in [80,100]$°C
$T_{jm\_conv} \in [100,120]$°C

Figures 4.6-4.9 show the average LPF for different power factors operating at the whole studied loading range.



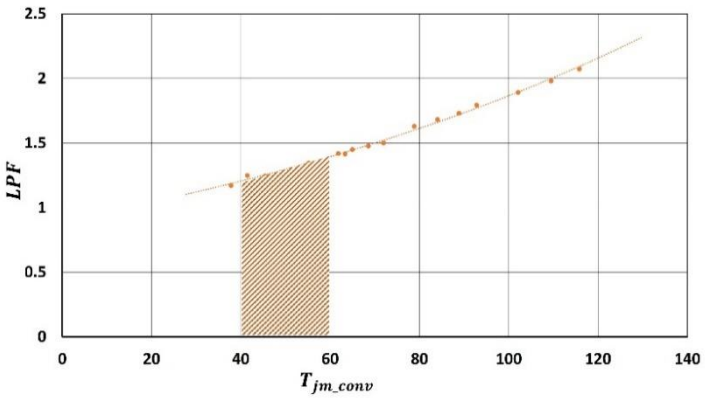
$\frac{1}{20}\int_{40}^{60} 0.5904e^{0.0118x}\,dx$ = 1.067

(a)



$\frac{1}{20}\int_{40}^{60} 0.7225e^{0.0099x}\,dx$ = 1.187

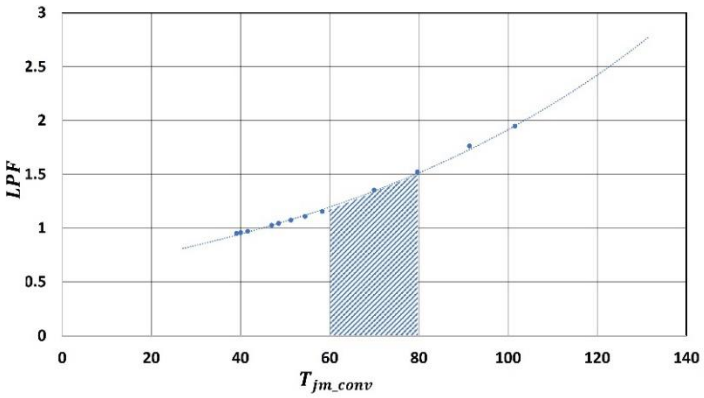
(b)



$\frac{1}{20}\int_{40}^{60} 0.9014e^{0.0073x}\,dx$ = 1.2995

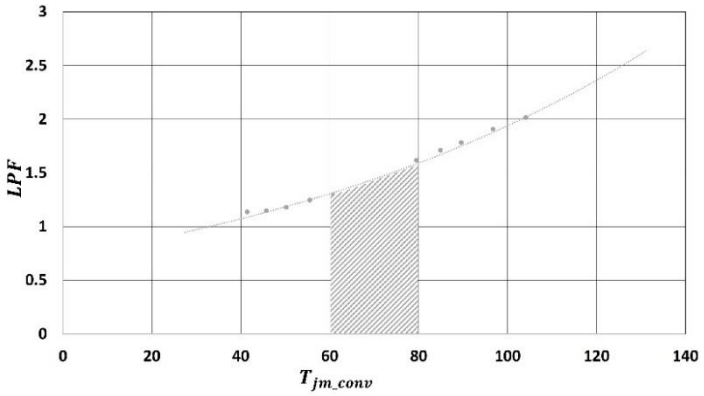
(c)

Figure 4.6: The average LPF for a loading range of T_{jm_conv}°C ∈ [40,60] for (a) PF = 0.6, (b) PF = 0.78, (c) PF = 0.97



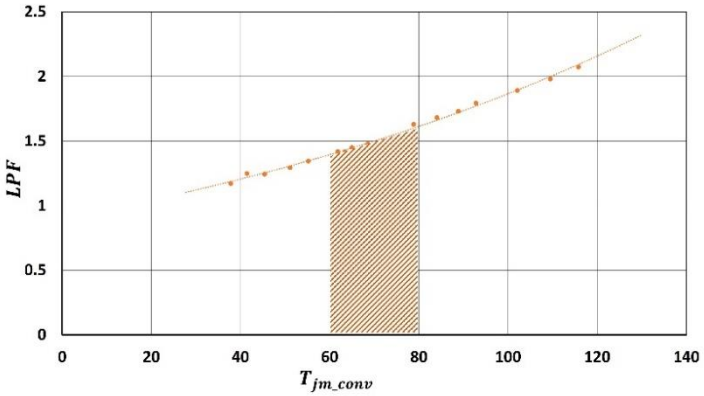
$$\frac{1}{20}\int_{60}^{80} 0.5904e^{0.0118x}\,dx = 1.3515$$

(a)



$$\frac{1}{20}\int_{60}^{80} 0.7225e^{0.0099x}\,dx = 1.447$$

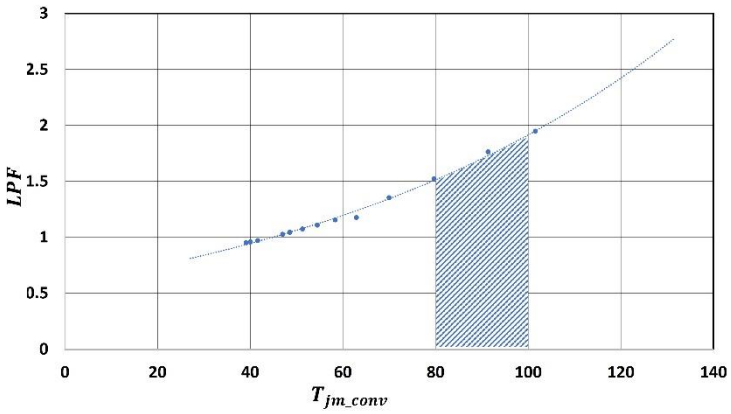
(b)



$$\frac{1}{20}\int_{60}^{80} 0.9014e^{0.0073x}\,dx = 1.504$$

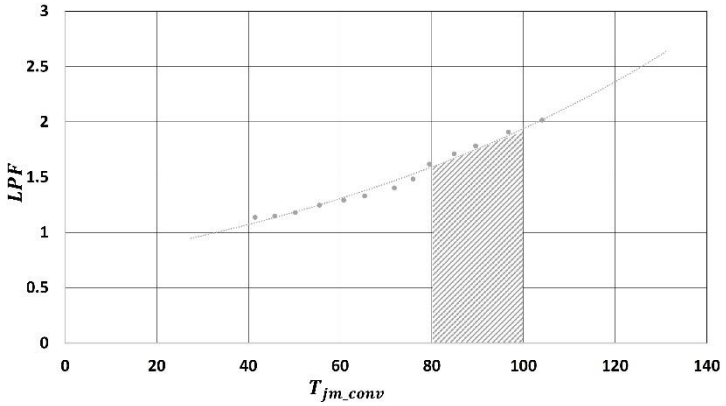
(c)

Figure 4.7: The average LPF for a loading range of T_{jm_conv}°C ∈ [60,80] for (a) PF = 0.6, (b) PF = 0.78, (c) PF = 0.97



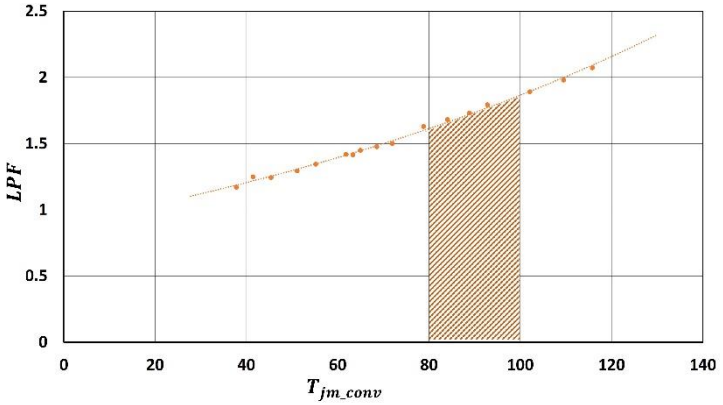
$$\frac{1}{20}\int_{80}^{100} 0.5904e^{0.0118x}\,dx = 1.7115$$

(a)



$$\frac{1}{20}\int_{80}^{100} 0.7225e^{0.0099x}\,dx = 1.764$$

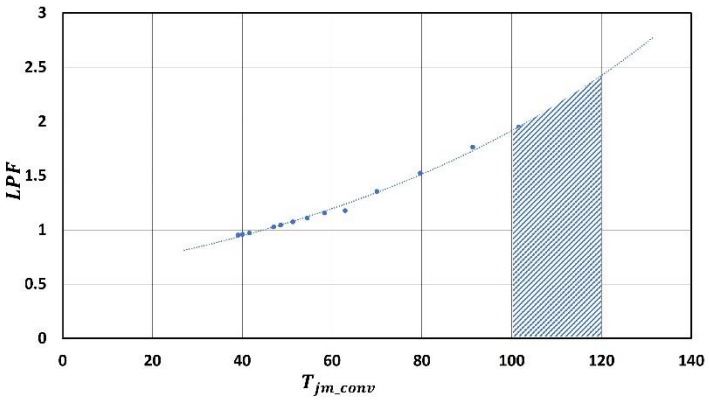
(b)



$$\frac{1}{20}\int_{80}^{100} 0.9014e^{0.0073x}\,dx = 1.7405$$

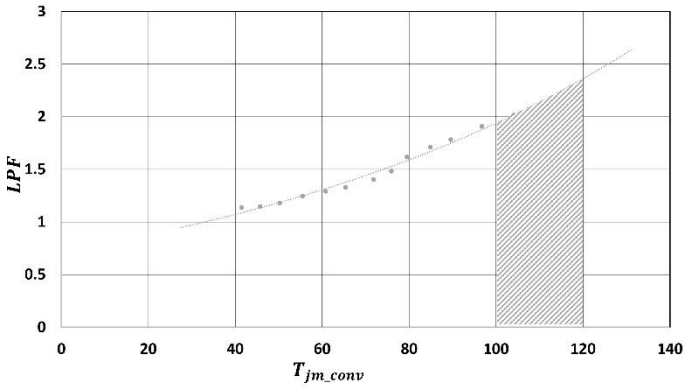
(c)

Figure 4.8: The average LPF for a loading range of T_{jm_conv}°C ∈ [80,100] for (a) PF = 0.6, (b) PF = 0.78, (c) PF = 0.97



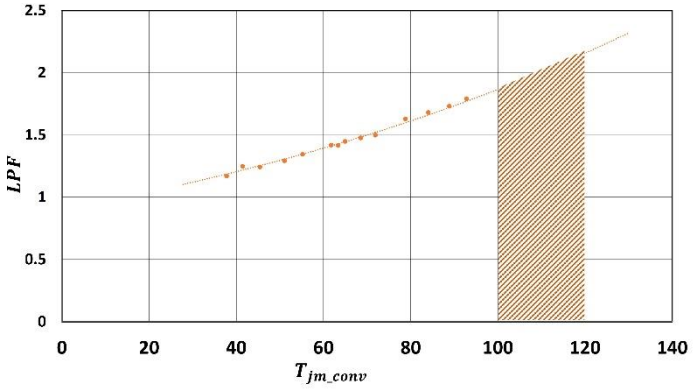
$\frac{1}{20}\int_{100}^{120} 0.5904e^{0.0118x}\,dx = 2.167$

(a)



$\frac{1}{20}\int_{100}^{120} 0.7225e^{0.0099x}\,dx = 2.150$

(b)



$\frac{1}{20}\int_{100}^{120} 0.9014e^{0.0073x}\,dx = 2.014$

(c)

Figure 4.9: The average LPF for a loading range of T_{jm_conv}°C ∈ [100,120] for (a) PF = 0.6, (b) PF = 0.78, (c) PF = 0.97

In conclusion, Figure 4.6 and Figure 4.7, show the trendlines of the LPF with respect to T_{jm_conv} for all three power factors, with a focus on the lower load range namely, $T_{jm\_conv} \in [40,80]$.

It was found that the case with the highest power factor is superior to the lower power factor cases. On the other hand, Figure 4.8 represented the closest results among all power factor values, compared to other levels of loading, where all three power factor values have close average LPF within $T_{jm\_conv} \in [80,100]$ with a slight advantage for the medium power factor value. Finally, Figure 4.9 shows that at higher loads, the superiority goes to the lowest power factor, since it incorporated the highest average LPF.

Figure 4.10 shows that higher loading levels are preferable to apply the proposed double switch H-bridge topology in general. However, at high loading levels, low power factors have better performance than high power factors. On the other hand, at low loading levels, high power factors have better performance than low power factors.

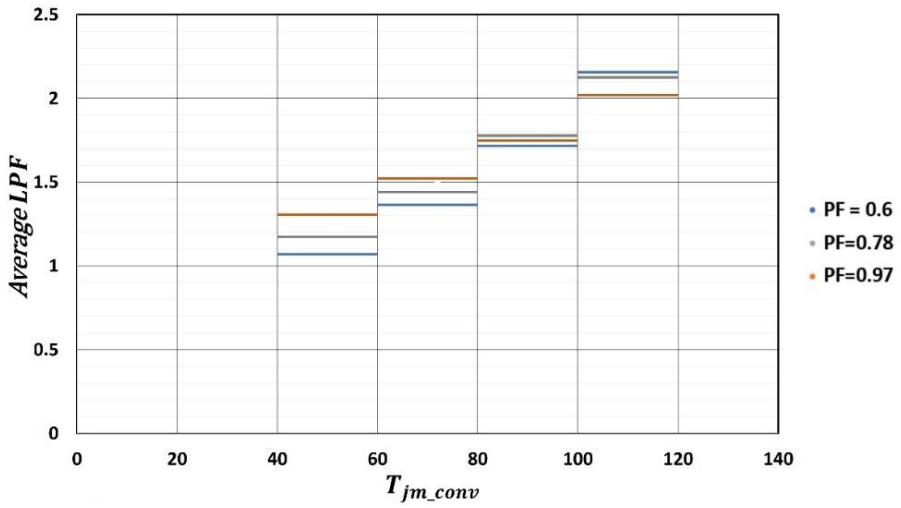


Figure 4.10: Average LPF for all power factors throughout the full loading ranges

4.5 Chapter Summary

This chapter presents the results of comparison between the double switch proposed topology and the conventional topology when sinusoidal Unipolar PWM modulation technique is applied to both. Three values of Power Factor were considered to represent the common loads' nature namely, Low PF, Medium PF, and High PF. Each power factor was individually simulated using PLECS® across the full expected thermal loading range of semiconductors (represented by the median junction temperature T_{jm}°C). Furthermore, the relationship between the $\%T_{jm\_red}$ and $\%\Delta T_{j\_red}$ (resulting from adopting the proposed topology) with the semiconductors lifetime improvement is evaluated using the lifetime improvement evaluation curve previously developed in Chapter 3.

Finally, a detailed comprehensive discussion compares the two topologies at low, medium, and high power factors, covering adequate loading levels for each power factor value. The resultant average Life-Prolonging Factor (LPF) was deduced for each individual case; hence, the performance of the proposed topology is validated and compared with the conventional method at numerous identical loading conditions, proving the superiority of the proposed topology over the conventional method in terms of reliability in the vast majority of conditions.

Chapter 5: Conclusions and Recommendations

5.1 Overall Conclusions

This thesis presents the development of a double switch topology for single-phase inverters intending to benefit most of the inverters' applications in terms of reliability. This research has two objectives, namely, (1) to develop an effective inverter topology that can effectively boost the expected lifetime of power switches, (2) to validate the proposed topology's performance through a suitable empirical-based lifetime estimation model.

To accomplish the first objective, a novel double switch topology is developed. For this study, the simulations and the proof-of-concept are simulated using MATLAB® and PLECS® software. The instantaneous junction temperatures of IGBT power switches are measured and recorded for numerous loading conditions. Important features were extracted from the instantaneous junction temperatures waveforms, such as the junction's median temperature T_{jm}, the junction's temperature swing ΔT_j, and the thermal cycling frequency for each topology f_c. These features are essential for evaluating the power switches' tendency to fail over time and estimating their lifetime.

To achieve the second objective, an empirical lifetime estimation model was considered to evaluate and compare the estimated lifetime of the two topologies at identical loading conditions. The models were manipulated to produce a novel lifetime improvement evaluation curve, which can be even used to describe the effect of any change in T_{jm}°C or ΔT_j on the estimated lifetime of power switches. This novel lifetime improvement evaluation curve can help in future studies to visualize the effect of the cooling system on the expected lifetime. Moreover, tests were conducted to cover a

variety of power factors and loading levels while comparing the two topologies. The test results indicate that the proposed topology can significantly improve the reliability in contrast with the conventional inverter topology.

All of the research objectives are met, and the results are robust and effective. The development of the proposed technique in this research fulfills the perpetually growing need to design more reliable power converters. This research work can easily and effectively be mapped and re-evaluated with great potential for vast power electronics applications, such as three-phase inverters and DC-DC Buck/Boost converters.

5.2 Significant Contributions of the Research

The significant contribution of this thesis can be summarized as follows:

i. Currently, no research has proposed a topology to enhance the lifetime of power switches with validation experiments. Therefore, the double switch H-bridge inverter topology is a novel topology for reliability enhancement.
ii. A novel lifetime improvement evaluation curve is developed to directly assess the effect of T_{jm}°C and ΔT_j changes on the lifetime of power switches. The lifetime improvement evaluation curve can be used in studies aiming to optimize the cooling systems of any power converter in terms of the system's overall reliability. The developed code can be easily tweaked to suit elements other than power switches, as long as their primary failure inducer is thermal cycling.

5.3 Recommendations for Future Studies

This thesis presents an inverter topology to enhance the lifetime of the inverter's power switches. However, the following future studies are suggested for further development:

i. The adopted modulation technique was a modified version of the sinusoidal Unipolar PWM technique. Other modulation techniques can be validated using the double switch proposed topology, and their impact on reliability can be assessed and compared to the results of this thesis.
ii. An actual module-heatsink thermal interface can be extracted and used in the thermal simulation as the RC network to better show the impact of the topology on the power switches' lifetime.
iii. In the same manner -as they were used in this study- double switches topology can be applied to other power converters such as three-phase converters and DC-DC Buck/Boost converters serving different applications. Reliability assessment can then be performed on different operational scenarios of the converters.
iv. A dedicated effort can be put aiming to reduce ΔT_j when the proposed topology is applied, which would boost the effectiveness of the topology even more.

References

[1] X. Wang, A. Castellazzi, and P. Zanchetta, “Regulated cooling for reduced thermal cycling of power devices,” in *IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia, IPEMC 2012*, 2012, vol. 1, pp. 238-244.

[2] D. A. Murdock, J. E. Ramos, J. J. Connors, and R. D. Lorenz, “Active Thermal Control of Power Electronics Modules,” in *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, 2003, vol. 3, pp. 1511-1515.

[3] X. Wang, A. Castellazzi, and P. Zanchetta, "Temperature control for reduced thermal cycling of power devices," in 2013 *15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-10.

[4] M. Weckert, and J. Roth-Stielow, "Lifetime as a control variable in power electronic systems," in *2010 Emobility - Electrical Power Train*, 2010, pp. 1-6.

[5] B. K. Bose, "Global Energy Scenario and Impact of Power Electronics in 21st Century," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2638-2651, 2013.

[6] British Petroleum Cp, "Bp Statistical Review of World Energy 2021", London, UK, 2021. Retrieved January 20, 2022, from https://www.bp.com/en/global/corporate/energy-economics/statistical-review-of-world-energy.html

[7] L. M. Moore, and H. N. Post, “Five years of operating experience at a large, utility-scale photovoltaic generating plant,” *Progress in Photovoltaics: Research and Applications*, vol. 16, no. 3, pp. 249-259, 2008.

[8] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 33-44.

[9] M. G. Pecht, and Ed., “Handbook of Electronic Package Design,” *New York: Marcel Dekker*, https://doi.org/10.1201/9781315214085, 1991.

[10] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-Failure Lifetime Prediction Models for Wire Bond Interconnects in Power Electronic Modules," *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 1, pp. 9-17, 2013.

[11] A. Nejadpak, and O. A. Mohammed, "A physics-based, dynamic electro-thermal model of silicon carbide power IGBT devices," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 201-206.

[12] J. McPherson, “Reliability Physics and Engineering,” 2nd ed. *Switzerland: Springer Int*, https://doi.org/10.1007/978-3-319-93683-3, 2013.

[13] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734-2752, 2010.

[14] J. M. Anderson, R. W. Cox, and P. O'Connor, "Online algorithm for early stage fault detection in IGBT switches," in *2013 9th IEEE International Symposium on Diagnostics for Electric Machines, Power Electronics and Drives (SDEMPED)*, 2013, pp. 1-8.

[15] A. Hanif, Y. Yu, D. DeVoto, and F. Khan, "A Comprehensive Review Toward the State-of-the-Art in Failure and Lifetime Predictions of Power Electronic Devices," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4729-4746, 2019.

[16] M. Ciappa, and W. Fichtner, "Lifetime prediction of IGBT modules for traction applications," in *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059)*, 2000, pp. 210-216.

[17] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol 42, no 4-5, pp. 652-667, 2002.

[18] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of Bond Wire Fatigue of IGBTs in a PV Inverter Under a Long-Term Operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7171-7182, 2016.

[19] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proceedings of Second International Conference on Power Electronics and Drive Systems*, 1997, pp. 425-430.

[20] E. Herr, T. Frey, R. Schlegel, A. Stuck, and R. Zehringer, "Substrate-to-base solder joint reliability in high power IGBT modules," *Microelectronics Reliability*, vol. 37, no. 10-11, pp. 1719-1722, 1997.

[21] T. Nguyen, S. Lefebvre, P.-Y. Joubert, D. Labrousse, and S. Bontemps, "Estimating Current Distributions in Power Semiconductor Dies Under Aging Conditions: Bond Wire Liftoff and Aluminum Reconstruction," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 4, pp. 483-495, 2015.

[22] J. D. Kraus, "Electromagnetics". *New York: McGraw-Hill*, https://doi.org/10.1063/1.3061617, 1953.

[23] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, vol. 98, no. 12, p. 121301, https://doi: 10.1063/1.2147714, 2005.

[24] G. H. Buh, H. J. Chung, and Y. Kuk, "Real-time evolution of trapped charge in a SiO2 layer: An electrostatic force microscopy study," *Applied Physics Letters*, vol. 79, no. 13, pp. 2010-2012, 2001.

[25] J. Suehle, P. Chaparala, C. Messick, W. Miller, and K. Boyko, “Field and Temperature Acceleration of Time-Dependent Dielectric Breakdown in Intrinsic Thin SiO2,” in *IEEE International Reliability Physics Symposium*, 1994, https://doi.org/10.1557/PROC-386-227.

[26] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, “Precursor Parameter Identification for Insulated Gate Bipolar Transistor (IGBT) Prognostics,” *IEEE Transactions on Reliability*, vol. 58, no. 2, pp. 271-276, 2009.

[27] N. Ren, K. L. Wang, J. Wu, H. Xu, and K. Sheng, "Failure Mechanism Analysis of SiC MOSFETs in Unclamped Inductive Switching Conditions," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 183-186.

[28] L. Benbahouche, A. Merabet, and A. Zegadi, "A comprehensive analysis of failure mechanisms: Latch up and second breakdown in IGBT(IXYS) and improvement," in *2012 19th International Conference on Microwaves, Radar & Wireless Communications*, 2012, pp. 190-192.

[29] K. Ramakrishna, and R. S. W. Lee, “Prognostics and health management of electronics,” *IEEE Transactions on Components and Packaging Technologies*, vol. 29, no. 1, pp. 3-4, 2006.

[30] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, “Condition Monitoring: A Decade of Proposed Techniques,” *IEEE Industrial Electronics Magazine*, vol. 9, no. 4, pp. 22-36, 2015.

[31] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, “Catastrophic failure and fault-tolerant design of IGBT power electronic converters - An overview,” in *IECON Proceedings (Industrial Electronics Conference)*, 2013, pp. 507-513.

[32] J. Due, S. Munk-Nielsen, and R. Nielsen, "Lifetime investigation of high power IGBT modules," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-8.

[33] S. Kalker, "Reviewing Thermal-Monitoring Techniques for Smart Power Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 2, pp. 1326-1341, 2022.

[34] B. Bidouche, Y. Avenas, M. Essakili, and L. Dupont, "Thermal characterization of an IGBT power module with on-die temperature sensors," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 2317-2322.

[35] J. Brandelero, J. Ewanchuk, and S. Mollov, “Online junction temperature measurements for power cycling power modules with high switching frequencies,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2016, vol. 2016, pp. 191-194.

[36] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature estimator for active thermal control," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7.

[37] U. Franke, R. Krümmer, T. Reimann, J. Petzoldt, and L. Lorenz, "Online monitoring of power devices junction temperature in power converters using a 32-bit microcontroller," in *Proceedings of the IEEE International Conference on Industrial Technology*, 2003, vol. 2, pp. 1130-1134.

[38] Y. Yu, T. Y. T. Lee, and V. A. Chiriac, "Compact thermal resistor-capacitor-network approach to predicting transient junction temperatures of a power amplifier module," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 7, pp. 1172-1181, 2012.

[39] F. Christiaens, B. Vandevelde, E. Beyne, R. Mertens, and J. Berghmans, "A Generic methodology for deriving compact dynamic thermal models, applied to the PSGA package," *IEEE transactions on components, packaging, and manufacturing technology. Part A*, vol. 21, no. 4, pp. 565-576, 1998.

[40] J. Palacin, M. Salleras, M. Puig, J. Samitier, and S. Marco, "Evolutionary algorithms for compact thermal modelling of microsystems: Application to a micro-pyrotechnic actuator," *Journal of Micromechanics and Microengineering*, vol. 14, no. 7, pp. 1074-1082, 2004.

[41] M. Salleras, "A methodology to extract dynamic compact thermal models under time-varying boundary conditions: Application to a thermopile based IR sensor," *Microsystem Technologies*, vol. 12, no. 1-2 SPEC. ISS., pp. 21-29, 2005.

[42] M. Janicki, M. Zubert, and A. Napieralski, "Generation of reduced thermal models of electronic systems from transient thermal response," in *2011 12th Intl. Conf. on Thermal, Mechanical & Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, 2011, pp. 1/4-4/4.

[43] G. L. Skibinski, and W. A. Sethares, "Thermal parameter estimation using recursive identification," in *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, 1990, no. pt 2, pp. 1581-1588.

[44] T.-Y. T. Lee, V. A. Chiriac, and R. Stout, "A conjugate numerical-rc network prediction of the transient thermal response of a power amplifier module in handheld telecommunication," in *ASME/Pacific Rim Tech. Conf. Exhibit. Integr. Packag. MEMS, NEMS, Electron. Syst.*, 2005, pp. 105-112.

[45] Infineon, "Transient thermal measurements and thermal equivalent circuit models." Retrieved February 15, 2022, from https://www.infineon.com.

[46] H. Vinke, and C. Lasance, "Thermal Characterization of Electronic Devices by Means of Improved Boundary Condition Independent Compact Models," *Thermal Management of Electronic Systems II*, pp. 115-124, 1997.

[47] T. Bechtold, E. B. Rudnyi, and J. G. Korvink, “Dynamic Electro-Thermal Simulation of Microsystems-a Review Electro-Thermal Simulation of Microsystems-a Review,” *J. Micromech. Microeng.*, vol. 15, no. 11, pp. R17-R31, 2005.

[48] R. Wu, “A Temperature-Dependent Thermal Model of IGBT Modules Suitable for Circuit-Level Simulations,” *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3306-3314, 2016.

[49] H. Lim, J. Hwang, S. Kwon, H. Baek, J. Uhm, and G. Lee, “A study on real time igbt junction temperature estimation using the ntc and calculation of power losses in the automotive inverter system,” *Sensors*, vol. 21, no. 7, https://doi.org/10.3390/s21072454, 2021.

[50] B. Cougo, L. M. F. Morais, G. Segond, R. Riva, and H. T. Duc, “Influence of PWM Methods on Semiconductor Losses and Thermal Cycling of 15-kVA Three-Phase SiC Inverter for Aircraft Applications,” *Electronics (Switzerland)*, vol. 9, no. 4, https://doi.org/10.3390/electronics9040620, 2020.

[51] F. Forest, “Use of opposition method in the test of high-power electronic converters,” *IEEE Transactions on Industrial Electronics*, vol. 53, no. 2, pp. 530-541, 2006.

[52] B. Cougo, H. Schneider, and T. Meynard, "Accurate switching energy estimation of wide bandgap devices used in converters for aircraft applications," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-10.

[53] A. M. Hava, “Carrier Based Pwm-Vsi Drives In The Overmodulation Region,” Ph.D. dissertation, Dept. Elect. Eng., University of Wisconsin – Madison, July, 1998, Retrieved March 15, 2022, from https:// https://ieeexplore.ieee.org/document/704136.

[54] B. Cougo, T. A. Meynard, F. Forest, and E. Labouré, “Optimal PWM method for flux reduction in InterCell Transformers coupling double three-phase systems,” *European Journal of Electrical Engineering*, vol. 15, https://doi: 10.3166/ejee.15.23-38, 2010.

[55] A. M. Hava, R. J. Kerkman, and T. A. Lipo, “Simple analytical and graphical tools for carrier based PWM methods,” in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 1997, vol. 2, pp. 1462-1471.

[56] P. Liu, J. Xu, Y. Yang, H. Wang, and F. Blaabjerg, “Impact of Modulation Strategies on the Reliability and Harmonics of Impedance-Source Inverters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 3968-3981, 2020.

[57] N. H. Baars, C. G. E. Wijnands, and J. L. Duarte, “Reduction of thermal cycling to increase the lifetime of MOSFET motor drives,” in *IECON Proceedings (Industrial Electronics Conference)*, 2014, pp. 1740-1746.

[58] A. Soldati, F. Dossena, G. Pietrini, D. Barater, C. Concari, and F. Iannuzzo, “Thermal stress mitigation by Active Thermal Control: Architectures, models and specific hardware,” in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 3822-3829.

[59] Y. Sakai, D. Oya, S. Iura, K. Ota, K. Hatori, and E. Stumpf, “Power cycle lifetime improvement by reducing thermal stress of a new dual HVIGBT module,”, in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1-7.

[60] X. Wang, Y. Wang, and A. Castellazzi, “Reduced active and passive thermal cycling degradation by dynamic active cooling of power modules,” in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2015, vol. 2015-June, pp. 309-312.

[61] L. Wei, J. Mcguire, and R. A. Lukaszewski, “Analysis of PWM frequency control to improve the lifetime of PWM inverter,” in *2009 IEEE Energy Conversion Congress and Exposition, ECCE 2009*, 2009, pp. 900-907.

[62] U.-M. Choi, I. Vernica, and F. Blaabjerg, “Asymmetric Pulse Width Modulation for Improving the Reliability of Motor Drive Inverters,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6430-6435.

[63] J. W. Kolar, H. Ertl, and F. C. Zach, “Influence of the Modulation Method on the Conduction and Switching Losses of a PWM Converter System,” *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063-1075, 1991.

[64] F. Zaamouche, S. Saad, and L. Hamiche, “A Discontinuous PWM Techniques Evaluation by Analysis of Voltage and Current Waveforms,” *International Jounral of Scientific Research and Engineering Technology (IJSET)*, pp. 8-13, 2019.

[65] O. Ojo, “The generalized discontinuous PWM scheme for three-phase voltage source inverters,” *IEEE Transactions on Industrial Electronics*, vol. 51, no. 6, pp. 1280-1289, 2004.

[66] A. M. Hava, R. J. Kerkman, and T. A. Lipo, “A high-performance generalized discontinuous PWM algorithm,” *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059-1071, 1998.

[67] J. W. Kolar, H. Ertl, and F. C. Zach, "Minimizing the current harmonics RMS value of three-phase PWM converter systems by optimal and suboptimal transition between continuous and discontinuous modulation," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, 1991, pp. 372-381.

[68] K. Taniguchi, Y. Ogino, and H. Irie, “PWM Technique for Power MOSFET Inverter,” *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 328-334, 1988.

[69] M. Khalid, A. Mohan, and A. C. Binojkumar, “Performance Analysis of Vector controlled PMSM Drive modulated with Sinusoidal PWM and Space Vector PWM,”, in *2020 IEEE International Power and Renewable Energy Conference*, 2020, https://doi: 10.1109/IPRECON49514.2020.9315210, 2020.

[70] Y. Y. Jia, X. D. Wang, L. L. Mao, S. C. Yang, and H. X. Zhang, “Application and simulation of SVPWM in three phase inverter,” in *Proceedings of the 6th International Forum on Strategic Technology, IFOST 2011*, 2011, vol. 1, pp. 541-544.

[71] B. Tan, Z. Gu, K. Shen, and X. Ding, “Third harmonic injection SPWM method based on alternating carrier polarity to suppress the common mode voltage,” *IEEE Access*, vol. 7, pp. 9805-9816, 2019.

[72] S. Albatran, A. S. Allabadi, A. R. Al Khalaileh, and Y. Fu, “Improving the Performance of a Two-Level Voltage Source Inverter in the Overmodulation Region Using Adaptive Optimal Third Harmonic Injection Pulsewidth Modulation Schemes,” *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 1092-1103, 2021.

[73] A. Ibrahim, and M. Z. Sujod, "The Impact of Variable DC-Bus Voltage Control on the Inverter Lifetime in Electric Vehicle Applications," in *2020 IEEE Symposium on Industrial Electronics & Applications (ISIEA)*, 2020, pp. 1-6.

[74] M. Andresen, K. Ma, G. de Carne, G. Buticchi, F. Blaabjerg, and M. Liserre, “Thermal Stress Analysis of Medium-Voltage Converters for Smart Transformers,” *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4753-4765, 2017.

[75] J. Zhang, G. Chen, and X. Cai, "Thermal smooth control for Multi-MW parallel wind power converter," in *2013 IEEE International Conference of IEEE Region 10 (TENCON 2013)*, 2013, pp. 1-4.

[76] J. Lemmens, P. Vanassche, and J. Driesen, “Optimal Control of Traction Motor Drives Under Electrothermal Constraints,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 2, pp. 249-263, 2014.

[77] S. Yin, Y. Wang, T. Yin, C. Nie, G. Duan, and Z. Wang, “Instantaneous Power Loss Calculation for MMC Based on Virtual Arm Mathematical Model,” in *2018 International Power Electronics Conference, IPEC-Niigata - ECCE Asia 2018*, 2018, pp. 2625-2629.

[78] J. N. Davidson, D. A. Stone, and M. P. Foster, "Real-time temperature monitoring and control for power electronic systems under variable active cooling by characterisation of device thermal transfer impedance," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, 2014, pp. 1-6.

[79] W. J. Choy, A. Castellazzi, and P. Zanchetta, "Adaptive cooling of power modules for reduced power and thermal cycling," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-10.

[80] R. Schacht, B. Wunderle, E. Auerswald, B. Michel, and H. Reichl, "Accelerated Active High-Temperature Cycling Test for Power MOSFETs," in *Thermal and Thermomechanical Proceedings 10th Intersociety Conference on Phenomena in Electronics Systems, 2006. ITHERM 2006.*, 2006, pp. 1102-1110.

[81] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1-6.

[82] D. Hirschmann, D. Tissen, S. Schröder, and R. W. de Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2511-2517, 2007.

[83] A. T. Bryant, P. A. Mawby, P. R. Palmer, E. Santi, and J. L. Hudgins, "Exploration of power device reliability using compact device models and fast electrothermal simulation," *IEEE Transactions on Industry Applications*, vol. 44, no. 3, pp. 894-903, 2008.

[84] M. Ikonen, "Power cycling lifetime estimation of IGBT power modules based on chip temperature modeling," Ph.D. dissertation, Lappeenranta Univ. Technol., Lappeenranta, Finland, December, 2012, Retrieved March 4, 2022, from https://lutpub.lut.fi/handle/10024/86334.

[85] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test for insulated gate bipolar transistor modules in traction application," *International Journal of Electronics*, vol. 86, no. 10, pp. 1193-1204. 1999.

[86] A. Syed, "Limitations of Norris-Landzberg equation and application of damage accumulation based methodology for estimating acceleration factors for Pb free solders," in *2010 11th International Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2010, https://doi:10.1109/ESIME.2010.5464546.

[87] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. de Doncker, "Reliability and Reliability Testing," *Semiconductor Power Devices: Physics, Characteristics, Reliability*, Eds. *Deutschland: Springer International Publishing*, pp. 489-581, 2018.

[88] "Rohm Semiconductors thermal models", Retrieved March 15, 2022, from https://www.rohm.com/products/sic-power-devices/sic-mosfet.

UAE UNIVERSITY MASTER THESIS NO. 2022:59

This thesis proposes and investigates an approach to reduce the thermal stress subjected to single phase inverters, which in return, increases the lifetime of switches. Hence, increases the reliability of the system. This thesis also proposes a better interpretation of a lifetime estimation model.

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