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A High Step-up Parallel Boost/Quasi-Z-Source PWM DC-DC Converter for Photovoltaic Applications

Mahdi Rezvanyvardom
Arak University, m-rezvanyvardom@araku.ac.ir

A HIGH STEP-UP PARALLEL BOOST/QUASI-Z-SOURCE PWM DC-DC CONVERTER FOR PHOTOVOLTAIC APPLICATIONS

Mohammad Matin Dezhdar [1], Mahdi Rezvanyvardom [2*], Farbod Setoudeh [3] ,
Ashkan horri [1], Mohammad Bagher Tavakoli [1],

[1] Department of Electrical Engineering, Arak Branch, Islamic Azad University, Arak, Iran
m-dezhdar@araku.ac.ir, ashkan.horri@srbiau.ac.ir, m-tavakoli@iau-arak.ac.ir

[2] Department of Electrical Engineering, Faculty of Engineering, Arak University, Arak, Iran
m-rezvanyvardom@araku.ac.ir

[3] Department of Electrical Engineering, Arak University of Technology, Arak, Iran
f.setoudeh@arakut.ac.ir

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دراسة جدوى للتطبيق المباشر لعائلتي ديب وجيورمال الأرض الجافة للتسخين في مباني قرية مويل

ملخص

تتمتع الشفرة في عملية الحراثة بأكبر قدر من التفاعل مع جزيئات التربة. إنه يسبب البلى لهذه القطعة ويقلل من عمرها المتوقع. يعتبر ارتداء أدوات الحراثة ذا أهمية كبيرة للمزارعين من حيث الجوانب الاقتصادية ، وعمليات خفض جودة الحرث ، وزيادة استهلاك الطاقة. تهدف هذه الدراسة إلى دراسة ارتداء خمس مواد بما في ذلك صفيحة st37 من الصلب (SST37) ، والصلب المجلفن (GAS) ، والألياف الزجاجية (GFRP) ، واثنان من الطلاء (أي نيتريد التيتانيوم نانويد (nano–TiN) وكربيد التنتالوم) (نانو– TaC)) عن طريق الاخرق في وسط البلازما للطبقة على الفولاذ التقليدي. تم اختبار هذه القطع في ثلاثة أنواع من قوام التربة الخفيفة والمتوسطة والثقيلة. لتقييم ارتداء الأدوات ، تم تطوير فول الصويا الدوار. تم تقييم مستوى تشغيل الشفرات في ثلاث خطوات من 500 متر وما مجموعه 1500 متر مع معيار لانقاص الوزن بسبب التدهور في تقييم العمليات المختبرية. كان هناك فرق كبير بين العلاجات المختلفة. النقطة المهمة في هذا البحث هي أن الشفرات المطلية بالنانو ، بفضل خصائصها الفائقة والأسطح الملساء ، تتمتع بأفضل أداء للتآكل. تبلغ مقاومة التآكل حوالي 7 أضعاف مقاومة الفولاذ المطلي ، 5.5 مرة من الفولاذ المجلفن. أظهرت الألياف الزجاجية مع ألياف البوليمر المقواة أداء جيدًا ضد الصلب العادي والمجلفن ضد التآكل.

Abstract

In this article, a novel DC-DC converter is proposed, which is derived from the parallel combination of a conventional boost converter and a Quasi-Z-Source converter. This converter benefits from the features of both mentioned converters. Compared to similar structures, the proposed converter has a suitable gain. This is due to the parallel combination of two voltage-boosting structures, namely boost and Quasi-Z-Source. The simple and linear circuit operation of the converter is another advantage. On the other hand, the control circuit of the converter is also simple and can be designed as PWM. Due to the Quasi-interleaved structure at the input of the proposed converter, the input current is divided between two input paths. This reduces the current stress on active and passive elements. The input filter inductor has a large value. Therefore, the input current of the converter is continuous, and the converter operates in CCM. Additionally, the input current ripple is improved, which is suitable for many applications. The ohmic losses of the elements are low due to the current division between parallel paths. Therefore, its efficiency is improved compared to similar structures. This article presents the design and performance analysis of the proposed converter. To validate the converter's performance, an 80-watt circuit was designed and simulated using PSPICE software. The comparison between the simulation results and the theoretical analysis of the proposed converter substantiates the accuracy of the proposed converter's operation.

Keywords: DC-DC converter, High step-up, Quasi-Z-Source converter, Boost converter, PWM.

1. INTRODUCTION

As fossil fuel resources continue to deplete, the significance of renewable energy sources in the industry has escalated. Among these renewable sources, solar cells stand out due to their ability to reduce environmental pollution and their widespread availability [1-3]. However, solar cells present a fundamental challenge: their output voltage is low, unstable, and unregulated due to varying environmental conditions. To overcome this, DC-DC boost converters are typically employed as intermediaries between the energy source and the consumer [5,6]. These converters, commonly used in the industry, generate a higher and regulated voltage level at the output. Nonetheless, boost converters have their own set of issues, such as limited voltage gain and output voltage dependency on the switch's duty cycle [7, 8]. As a result, a variety of techniques are routinely employed to enhance the voltage gain of the boost converter. Practical methods include the use of multiplier cells [9,10], coupled inductors [11,12], switched inductors [13], and switched capacitors [14]. Other strategies for augmenting voltage gain in DC-DC converters encompass series connection of converters [15,16], interleaving input inductors [17, 18], paralleling multiple voltage-boosting structures [19,20], and multilevel output voltage [21,22]. In the quest for stabilizing and increasing output voltage, Z-Source converters [23-25] have proven to be among the best. These converters simultaneously leverage the benefits of both current source converters and voltage source converters. The key advantages of current source converters include a reduction in the size of the output filter, elimination of instantaneous currents and voltages, a decrease in the ripple of the input current, and an increase in voltage gain. Conversely, voltage source converters offer benefits such as low impedance at the input source, effective control over the performance of switching elements, and the containment of transient currents [26].

A Z-Source converter proposed in [27] aimed to increase voltage gain. However, this converter falls short in terms of voltage gain and lacks a common ground between the input and output. This necessitates the use of floating ground gate drivers, leading to increased noise in the converter's operation. Given that the Z-Source converter lacks a common ground between the input and output, Quasi-Z-Source converters are typically utilized. A DC-DC converter, composed of boost cells and a Quasi-Z-Source converter, is introduced in [28] with the objective of amplifying the converter's voltage gain. However, this converter experiences high voltage stress on the switches and a high ripple current at the input. Moreover, the large number of active and passive elements in this converter leads to increased ohmic losses and reduced efficiency. In [29], a Quasi-Z-Source converter is proposed, which employs a resonant path to facilitate soft switching conditions and power transfer from input to output. The resonant operation of this converter results in escalated voltage and current stress on the circuit elements. Despite the incorporation of a voltage-boosting cell and a resonant cell, the voltage gain of the converter remains unsuitable for numerous applications. A Z-Source converter, which utilizes two symmetrical resonant circuits to enhance the voltage gain of the converter, is proposed in [30]. These two resonant circuits are situated in the power transfer path from the input to the output of the converter, leading to increased ohmic losses and consequently, reduced converter efficiency. Additionally, the operation of this converter is non-linear and complex. In [31], a novel Z-Source structure is proposed, which is combined with a network of switched inductors to improve the voltage gain of the converter. However, this converter has a complex structure and due to the presence of a large number of elements, it experiences high conduction losses. In [32], a Quasi-Z-Source converter is proposed that leverages both switched inductors and switched capacitors to enhance the voltage gain of the converter. This converter, however, faces issues such as the absence of a common ground between input and output, high voltage stress on switches and diodes, and discontinuous input current.

In this article, a new DC-DC converter is proposed that employs two parallel structures to enhance the linear operation of the circuit and increase the voltage gain. The first structure is a conventional boost converter, while the second structure is a Quasi-Z-Source converter. This converter shares a common ground between the input and output and does not necessitate a floating ground gate drive, resulting in less operational noise compared to Z-Source structures. This converter reaps the benefits of both current source and voltage converters. In the input section of the converter, a Quasi-interleaved structure is present, causing the input current to traverse two paths with different impedances, thereby reducing the current stress on the elements. Also, due to the large size of the input filter, which comprises input inductors and capacitors of the Quasi-Z-Source structure, the input current is continuous and exhibits low ripple. Consequently, this converter remains in the Continuous Conduction Mode (CCM) for a wide range of duty cycles. The operation of this converter is straightforward and similar to that of common boost and Quasi-Z-Source converters, thus exhibiting linear operation. The control circuit of the converter is also simple and is regulated by Pulse Width Modulation (PWM). Another notable feature of this converter is its high

voltage gain, which is suitable for a wide array of applications. This desirable voltage gain is attributed to the power transfer from two distinct paths towards the output. In order to investigate more accurately and with greater detail, this paper contains the following sections. The performance principle of the proposed converter is explained in section two. After that, small signal analysis is presented in section three. The simulation results are presented in section four. Finally, the conclusion is drawn in section five.

2. PRINCIPLES OF OPERATION

Figure 1 depicts the proposed parallel Boost/QZS DC-DC converter. This converter consists of a Quasi-network (inductors L1, L3, capacitors C1, C2, and diode D1), Boost inductor (L2), inductors (L4, L5,) that controls the current passing through the switching elements, two switches (S1, S2), two diodes (D2, D3), and an output capacitor (Co). The output voltage of the proposed converter is equal to the VCO. For analytical purposes, the proposed converter is assumed to have ideal elements, operates in continuous current mode (CCM), and operates in a steady-state condition. This simplifies the investigation by streamlining the complexity of the analysis. Figure 2 illustrates the theoretical waveforms of the proposed converter, which has four operating modes. The equivalent circuit for each operating mode is shown in Figure 3.

Mode 1(t_0<t<t_1, Figure 3(a))

At time (t0), this mode begins with the switch S1 turning on. Consequently, the current flowing through the inductor (L2) increases linearly. During this mode, the switch (S2) remains on, while the diode (D1) is off. Some of the energy stored in the capacitor (C2) is transferred to the inductor (L1), and other portions of stored energy in (C2) are transferred to the output via D2. Simultaneously, a portion of the stored energy in the capacitor (C1) is transferred to the inductor (L3), while the remaining energy is sent to the output. Additionally, the energy stored in the inductor (L4), via diode (D2), is also transferred to the output.

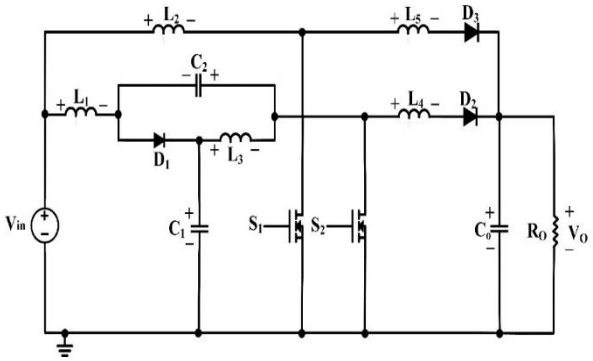

Figure 1. The proposed parallel Boost/QZS DC-DC converter

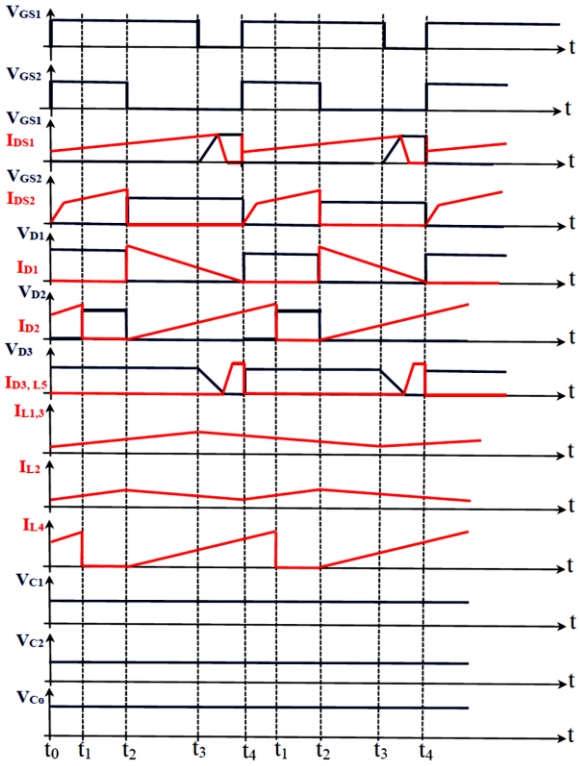

Figure 2. The theoretical waveforms of the proposed converter

$$V_{L2} = V_{in} = L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{1}$$

$$V_{L1} = V_{in} + V_{C2} = L_1 \frac{\Delta i_{L1}}{\Delta t} \tag{2}$$

$$\begin{cases} V_{L3} = V_{C1} = L_3 \dfrac{\Delta i_{L3}}{\Delta t} \\ V_{L4} = -V_o = L_4 \dfrac{\Delta i_{L4}}{\Delta t} \end{cases} \tag{3}$$

This mode concludes by transferring the entire stored energy from the inductor (L_4) to the output. Consequently, at (t = t_1), the current through the inductor (L_4) becomes zero, and diode (D_2) turns off under zero-current switching (ZCS).

$$\begin{cases} i_{L4}(t_0) = i_o \\ i_{L4}(t_1) = 0 \end{cases} \tag{4}$$

$$-V_O = L_4 \frac{0 - i_o}{t_1 - t_0} \Rightarrow t_1 - t_0 = \frac{L_4 i_o}{V_o} \tag{5}$$

$$\begin{cases} \Delta i_{L1} = \dfrac{V_{in}+V_{C2}}{V_o}\dfrac{L_4}{L_1} i_o \\ \Delta i_{L2} = \dfrac{V_{in}}{V_o}\dfrac{L_4}{L_2} i_o \\ \Delta i_{L3} = \dfrac{V_{C1}}{V_o}\dfrac{L_4}{L_3} i_o \end{cases} \quad (6)$$

Mode 2 (t_1<t<t_2, Figure 3(b))

At time (t_1), mode 2 starts by turning off the diode (D_2), while both switches remain on. Consequently, during this mode, power from the input is not transferred to the output. Instead, the capacitor (C_o) supplies the output. The status of all inductors and capacitors remains similar to that of mode 1.

$$i_{S2} = i_{L1} + i_{L3} \quad (7)$$

Mode 2 ends by turning off the switch (S_2) at t = t_2.

Mode 3 (t_2<t<t_3, Figure 3(c))

This mode commences by turning S_2 off at t = t_2. When S_2 turns off, as a result the diode D_2 turns on under ZCS. Simultaneously, D_1 also turns on. Consequently, the energy stored in L_1 is transferred to C_1, and the energy from L_3 is transferred to C_2. Similar to previous modes, the current through L_2 increases linearly.

$$V_{L1} = V_{in} - V_{C1} = L_1 \frac{\Delta i_{L1}}{\Delta t} \quad (8)$$

$$V_{L2} = V_{in} = L_1 \frac{\Delta i_{L1}}{\Delta t} \quad (9)$$

$$V_{L3} = -V_{C2} = L_3 \frac{\Delta i_{L3}}{\Delta t} \quad (10)$$

$$V_{L4} = V_{C1} + V_{C2} - V_o = L_4 \frac{\Delta i_{L4}}{\Delta t} \quad (11)$$

This mode ends by turning off S_1 at t=t_3.

Mode 4 (t_3<t<t_4, Figure 3(d))

This mode starts by turning off S_1 at t=t_3. By turning off S_1, the diode D_3 turns on under ZCS. Therefore, the energy stored in the inductor L_2 is transferred to the output.

$$L_{eq} = L_2 + L_5 \quad (12)$$

$$V_{Leq} = V_{in} - V_o = L_{eq} \frac{\Delta i_{L2}}{\Delta t} \quad (13)$$

It is feasible to ignore the value of the inductor L_5 in comparison to L_2. During this mode, the power is transferred from the input to the output through two parallel paths. By applying the concept of volt-second balance:

$$(D_1 + D_2)(V_{in} + V_{C2}) = (D_3 + D_4)(V_{C1} - V_{in}) \quad (14)$$

By using the volt-second balance to the inductor L_2:

$$(D_1 + D_2 + D_3)V_{in} = D_4(V_o - V_{in}) \quad (15)$$

$$V_{in} = D_4 V_o \Rightarrow M = \frac{V_o}{V_{in}} = \frac{1}{D_4} \quad (16)$$

$$t_4 - t_3 = D_4 T = \frac{V_{in}}{f V_o} \quad (17)$$

By using the volt-second balance to the inductor L_3:

$$(D_1 + D_2)V_{C1} = (D_3 + D_4)V_{C2} \quad (18)$$

$$\frac{V_{C1} - V_{in}}{V_{in} + V_{C2}} = \frac{V_{C2}}{V_{C1}} \quad (19)$$

$$V_{C2}^{\ 2} + V_{in}V_{C2} + V_{in}V_{C1} - V_{C1}^{\ 2} = 0 \quad (20)$$

By solving the above equation in term of V_{C2}:

$$V_{C2} = \frac{\sqrt{V_{in}^{\ 2} - 4(V_{in}V_{C1} - V_{C1}^{\ 2})} - V_{in}}{2} \quad (21)$$

By solving the above equation in term of V_{C1}:

$$V_{C1}^{\ 2} + V_{in}V_{C1} - (V_{in}V_{C2} + V_{C2}^{\ 2}) = 0 \quad (22)$$

$$V_{C1} = \frac{V_{in} + \sqrt{V_{in}^{\ 2} + 4(V_{in}V_{C2} + V_{C2}^{\ 2})}}{2} \quad (23)$$

By applying the volt-second balance to the inductor L_4:

$$D_1 V_o = (D_3 + D_4)(V_o - V_{C1} - V_{C2}) \quad (24)$$

$$D_3 + D_4 = \frac{D_1 V_o}{V_o - V_{C1} - V_{C2}} \quad (25)$$

Therefore, the time interval of mode 2 is equal to:

$$D_2 = \left[\frac{V_o(V_{C1} - V_{in})}{(V_{C2} + V_{in})(V_o - V_{C1} - V_{C2})} - 1 \right] D_1 \quad (26)$$

The time interval of mode 3 is equal to:

$$D_3 = 1 - D_1 - D_2 - D_4 \quad (27)$$

3. SMAL SIGNAL ANALYSIS

To evaluate the stability and performance of the proposed converter in open-loop mode, we utilize small signal analysis. The converter's behavior is assessed using averaged state-space modeling, applied across four distinct operating modes. It is crucial to note that in this context, both the voltages across the capacitors and the currents through the inductors are considered state variables. Furthermore, the analysis of the averaged state-space modeling for the proposed converter is specifically conducted under continuous conduction mode conditions. Generally, the state-space equations can be represented as follows:

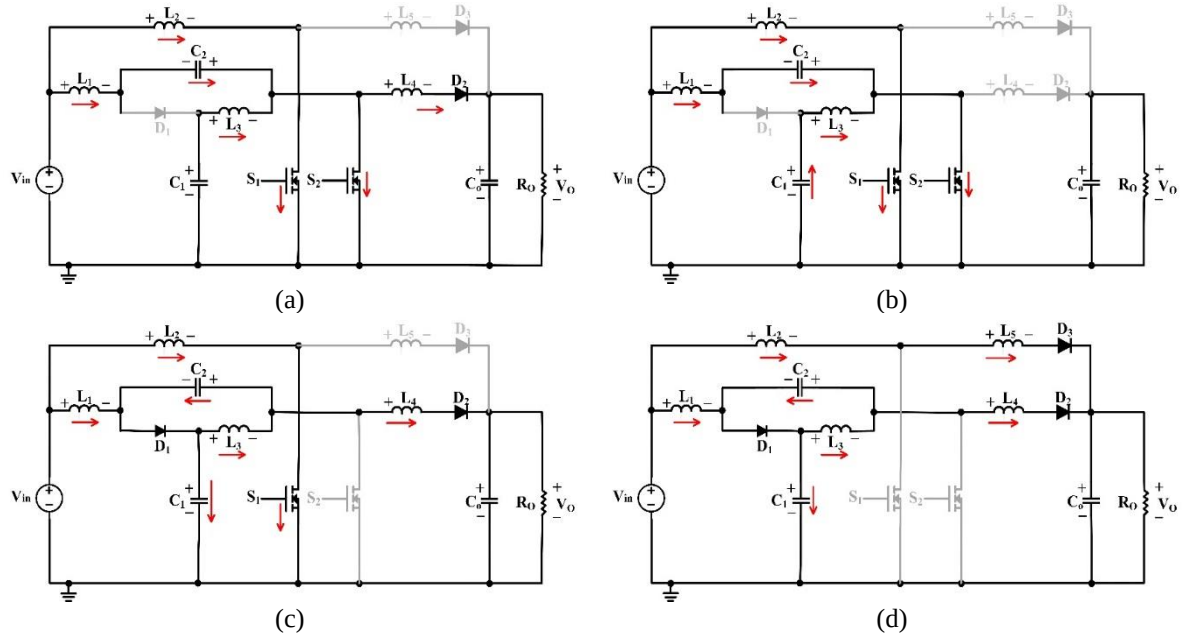

Figure 3. The equivalent circuit for each operating mode. (a) mode 1 [t_0-t_1], (b) mode 2 [t_1-t_2], (c) mode 3 [t_2-t_3], (d) mode 4 [t_3-t_4]

$$\begin{cases} \hat{x}(t) = A_j x(t) + Bu(t) \\ y(t) = C_j x(t) + Du(t) \end{cases} \quad (28)$$

In the context of these equations, (A_j) is defined as the state matrix, while (B) represents the input matrix. The output matrix is denoted by (C_j), and (D) stands for the input-output matrix. It is important to note that in this scenario, (j) signifies the operating mode number of the converter, which can take on the values of 1, 2, 3, or 4.

$$x(t) = \left[v_{C1}, v_{C2}, v_{CO}, i_{L1}, i_{L2}, i_{L3}, i_{L4}\right] \quad (29)$$

$$u(t) = \left[v_{in}, i_{in}\right] \quad (30)$$

$$y(t) = \left[v_o\right] \quad (31)$$

Based on the performance of the converter in its first mode, as illustrated in Figure 3(a), the state-space equations for this mode are as follows:

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{i_{L3}}{C_1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{i_{L1}}{C_2} \\ \dfrac{dv_{CO}}{dt} = \dfrac{i_{L4}}{C_O} - \dfrac{MV_{in}}{C_O R_O} \end{cases} \quad (32)$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{V_{in}}{L_1} + \dfrac{v_{C2}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{in}}{L_2} \\ \dfrac{di_{L3}}{dt} = \dfrac{v_{C1}}{L_3} \\ \dfrac{di_{L4}}{dt} = -\dfrac{MV_{in}}{L_4} \end{cases} \quad (33)$$

Considering the performance of the proposed converter in its second mode, we can derive the following equations:

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{i_{L3}}{C_1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{i_{L1}}{C_2} \\ \dfrac{dv_{CO}}{dt} = \dfrac{MV_{in}}{C_O R_O} \end{cases} \quad (34)$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{V_{in}}{L_1} + \dfrac{v_{C2}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{in}}{L_2} \\ \dfrac{di_{L3}}{dt} = \dfrac{v_{C1}}{L_3} \end{cases} \quad (35)$$

Analyzing the converter's performance in its third mode, as depicted in Figure 3(c), the corresponding state-space equations are presented below:

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{i_{in}}{C_1} - \dfrac{i_{L2}}{C_1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{i_{L3}}{C_2} - \dfrac{i_{L4}}{C_2} \\ \dfrac{dv_{CO}}{dt} = \dfrac{i_{L4}}{C_O} - \dfrac{MV_{in}}{C_O R_O} \end{cases} \quad (36)$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{V_{in}}{L_1} - \dfrac{v_{C1}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{in}}{L_2} \\ \dfrac{di_{L3}}{dt} = -\dfrac{v_{C2}}{L_3} \\ \dfrac{di_{L4}}{dt} = \dfrac{v_{C1}}{L_4} + \dfrac{v_{C2}}{L_4} - \dfrac{MV_{in}}{L_4} \end{cases} \quad (37)$$

Based on the performance of the proposed converter in mode 4, the state equations are as follows: It should be noted that due to the small amount of L_5, it is disregarded in the equations of this mode.

$$\begin{cases} \dfrac{dv_{C1}}{dt} = \dfrac{i_{in}}{C_1} - \dfrac{i_{L2}}{C_1} - \dfrac{i_{L4}}{C_1} \\ \dfrac{dv_{C2}}{dt} = \dfrac{i_{L3}}{C_2} - \dfrac{i_{L4}}{C_2} \\ \dfrac{dv_{CO}}{dt} = \dfrac{i_{L4}}{C_O} - \dfrac{MV_{in}}{C_O R_O} \end{cases} \quad (38)$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = \dfrac{V_{in}}{L_1} - \dfrac{v_{C1}}{L_1} \\ \dfrac{di_{L2}}{dt} = \dfrac{V_{in}}{L_2} - \dfrac{MV_{in}}{L_2} \\ \dfrac{di_{L3}}{dt} = -\dfrac{v_{C2}}{L_3} \\ \dfrac{di_{L4}}{dt} = \dfrac{v_{C1}}{L_4} + \dfrac{v_{C2}}{L_4} - \dfrac{MV_{in}}{L_4} \end{cases} \quad (39)$$

By employing the averaged state-space equations, we can determine the values of the matrices labeled A_{av} and B_{av}. The calculations are as follows:

$$\mathbf{A_{av}} = \begin{pmatrix} 0 & 0 & 0 & 0 & \frac{-D_3-D_4}{C_1} & \frac{D_1+D_2}{C_1} & \frac{-D_4}{C_1} \\ 0 & 0 & 0 & \frac{D_1+D_2}{C_2} & 0 & \frac{D_3+D_4}{C_2} & \frac{-D_3-D_4}{C_2} \\ 0 & 0 & \frac{-D_1+D_2-D_3}{C_O} & 0 & 0 & 0 & \frac{D_1+D_3}{C_O} \\ \frac{-D_3-D_4}{L_1} & \frac{D_1+D_2}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-D_4}{L_2} & 0 & 0 & 0 & 0 \\ \frac{D_1+D_2}{L_3} & \frac{-D_3-D_4}{L_3} & 0 & 0 & 0 & 0 & 0 \\ \frac{D_3+D_4}{L_4} & \frac{D_3+D_4}{L_4} & \frac{-D_1-D_3-D_4}{L_4} & 0 & 0 & 0 & 0 \end{pmatrix} \quad (40)$$

$$B_{av} = \begin{pmatrix} 0 & \frac{D_3 + D_4}{C_1} \\ 0 & 0 \\ 0 & 0 \\ \frac{D_1 + D_2 + D_3 + D_4}{L_1} & 0 \\ \frac{D_1 + D_2 + D_3 + D_4}{L_2} & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \quad (41)$$

In line with the principles outlined in the state-space equations, the open-loop transfer function of the proposed converter is derived from the given relationship.

$$G(s) = \frac{Y(s)}{u(s)} = C_{av}\left[SI - A_{av}\right]^{-1} B_{av} + D \quad (42)$$

The transfer function under consideration undergoes a thorough analysis using MATLAB software. Specifically, the Gzpk command is employed to determine its zeros and poles. This computational operation reveals that all zeros and poles associated with the open-loop transfer function of the proposed converter are located on the left-hand side of the S-Plane. This spatial distribution clearly indicates the system's stability, a desirable attribute that contributes to the robust performance of the converter under various operating conditions.

4. SIMULATION RESULTS

A prototype of the proposed parallel Boost/QZS DC-DC converter has been meticulously designed to operate at 80 watts. It is configured with an input voltage of 40V input and an output voltage 400V. Subsequently, a simulation was conducted using the PSPICE software to evaluate its performance. The converter operates at a switching frequency of 50 KHz for both of its main switches. In the Boost converter, to have a suitable voltage gain, D should be greater than 0.5. Therefore, D has been selected for 85%. On the other hand, in the QZS converter, having a voltage gain greater than one requires that D is smaller than 0.5. Therefore, D has been selected for 45%. In the design of this converter, the IRF250 switch is selected as switch S_1 due to its superior performance in the parallel boost circuit. Additionally, the IRFP240 switch is employed in the Quasi-Z-Source circuit. The diode D_1 is of the MUR840 type, while the output diodes are MUR460. Table 1 provides the parameters of this converter. Figure 4 illustrates the voltage and current waveforms associated with the switch S_1. According to the performance of the converter in the first mode, S_1 turns on at t = t_0. Given that this switch is connected in series with the inductor L_2, there is a linear increase in its current during this mode. Switch S_1 is related to the boost circuit in the proposed converter.

Table 1: Parameters of the proposed converter

The designed parameters for the proposed converter	value
Input Voltage (V_{in})	40 V
Output Voltage (V_{out})	400 V
Input inductor of Quasi-Z-Source converter (L_1)	5 mH
Input inductor of boost converter (L_2)	10 mH
Inductor (L_3)	5 mH
Output inductor of Quasi-Z-Source converter (L_4)	1 mH
Output inductor of boost converter (L_5)	1 µH
Capacitors (C_1, C_2)	2 mF
Output Capacitors (C_o)	100 µF

Similar to a conventional boost converter, the aim of turning on S_1 is to provide a pathway for energy storage in the inductor L_2. It's noteworthy that this switch remains on during three performance modes of the proposed converter. S_1 turns off at the beginning of mode 4. Therefore, similar to a conventional boost converter, the energy stored in the inductor L_2 is then transferred to the output of the converter.

The voltage and current waveforms corresponding to the switch S_2 are illustrated in Figure 5. This switch serves as the primary switch of the Quasi-Z-Source circuit and is turned on during the first mode. According to the performance of the converter in mode 1, the diode D_1 turns off when the switch S_2 turns on. As a result, the energy stored in the capacitors C_1 and C_2 is transferred to the L_3 and L_2, respectively. The activation of this switch provides the path for an increase in the current of the inductors L_1 and L_3. During this mode, the current of these inductors are increased linearly. Switch S_2 turns off at the beginning of mode 3. Consequently, a portion of the energy stored in the inductors L_1 and L_3 is transferred to the capacitors C_2 and C_1, respectively. The remaining energy is transferred to the output via the output diode. This operation behavior mirrors the performance of a conventional Quasi-Z-Source converter.

Figure 6 depicts the voltage and current waveforms for diode D_1. As per this figure and the operational characteristics of the proposed converter, diode D_1 is turned off when the switch S_2 is turned on, and conversely, it is turned on when the switch S_2 is turned off. At the onset of the third mode, with the deactivation of S_2, diode D_1 is turned on. This activation provides the transfer of energy from the inductors L_1 and L_3 to the capacitors C_1 and C_2,

respectively. Diode D_1 remains on during modes 3 and 4, enabling the transfer of energy from the input of the Quasi-Z-Source circuit to its output. It is turned off at the beginning of the first mode, a process governed by the observation of the volt-second balance in relation to L_1 and L_3. Turning off this diode provides the path for the transfer of energy from the capacitor C_1 to the inductors L_3 and L_1 via switch S_1. The waveforms of voltages and currents corresponding to the output diodes D2 and D3 are shown in Figure 7 and 8, respectively. Serving as the output diodes for both the Quasi-Z-Source circuit and the boost circuit, diodes D2 and D3 play a role in transferring power to the output.

Figure 9 presents the current waveform of the inductor L_1. According to the operation of the converter in modes 1 and 2, during these modes the current flowing through L_1 exhibits a linear increase. Concurrently, it stores energy derived from the input source and the capacitor C_2. According to the performance of the converter in CCM, the increase in the inductor`s current commences from a non-zero value. This inductor also serves the role of an input filter. During the operation of the converter in the third and fourth modes, the energy stored in this inductor is transferred to the capacitor C_1 and the output. Therefore, the current flowing through the inductor decreases linearly, returning to its initial non zero value. This process ensures the provision the volt-second balance. The waveform of the current flowing through the inductor L2 is illustrated in Figure 10. The performance of this inductor is similar to the input filter`s inductor in a conventional boost converter. By turning on the switch S1 during modes 1, 2, and 3, the energy is transferred from the input source to the inductor L2 resulting in a linear increase of its current. Given that the proposed converter operates in CCM, the initial current is not zero. By turning off the switch S1 during the fourth mode, the energy stored in the inductor L2 is transferred to the output, causing its current to decrease linearly.

The current waveform corresponding to the inductor L_3 is illustrated in Figure 11. When the switch S_2 is on, the energy stored in the capacitor C_1 is transferred to the inductor L_3. Throughout the operation of the converter, the voltages across the capacitors C_1 and C_2 undergo negligible fluctuations, causing a linear reduction in current until it stabilizes at a non-zero value. In accordance with the volt-second balance principle, when the switch S_2 is off, the energy stored in the capacitor C_2 is transferred to the inductor L_3, leading to a linear increase in its current.

Figure 12 depicts the current waveform associated with the inductor L_4 of the output filter in the Quasi-Z-Source circuit. In the first mode, the current flowing through the inductor L_4 decreases linearly due to the reverse output voltage across it. By the conclusion of this mode, the current reaches zero, signifying that all its energy has been transferred to the output. In the second mode, both the voltage and current of the inductor are equal to zero. During the third and fourth modes, the energy from the input source and energy stored in the components of the input section of the Quasi-Z-Source convertor lead to a linear increase in the current flowing through the inductor L_4.

The waveforms of the conventional capacitors C_1 and C_2 in the Quasi-Z-Source convertor are illustrated in Figure 13. The voltage across these capacitors does not exhibit a significant difference during their charging and discharging phases, given their values. Consequently, the voltages across these capacitors can be approximated as constant. This approximation is well corroborated by Figure 13.

The waveforms of the input and output voltages of the proposed convertor are shown in Figure 14. The presence of input and output filters in this converter ensures that the output voltage exhibits minimal ripple. Consequently, this characteristic enables the converter to operate effectively across a wide range of industrial applications.

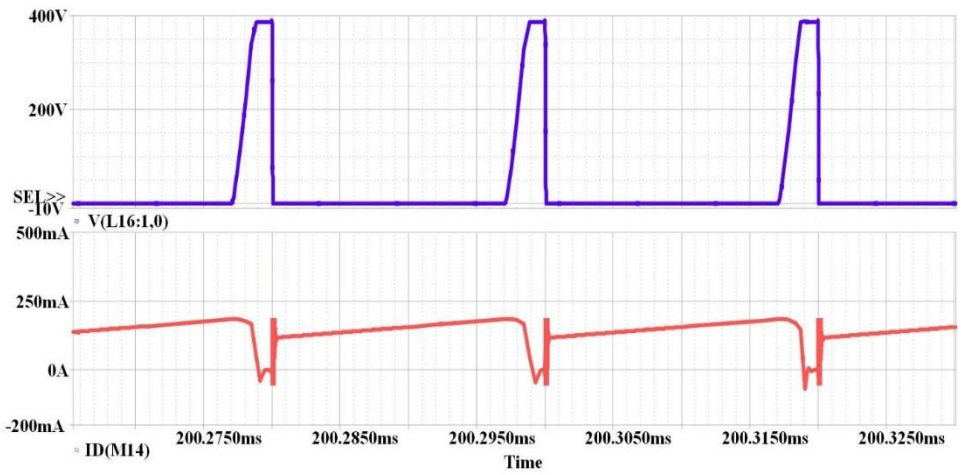

Figure 4. The voltage and current waveforms of the switch S_1

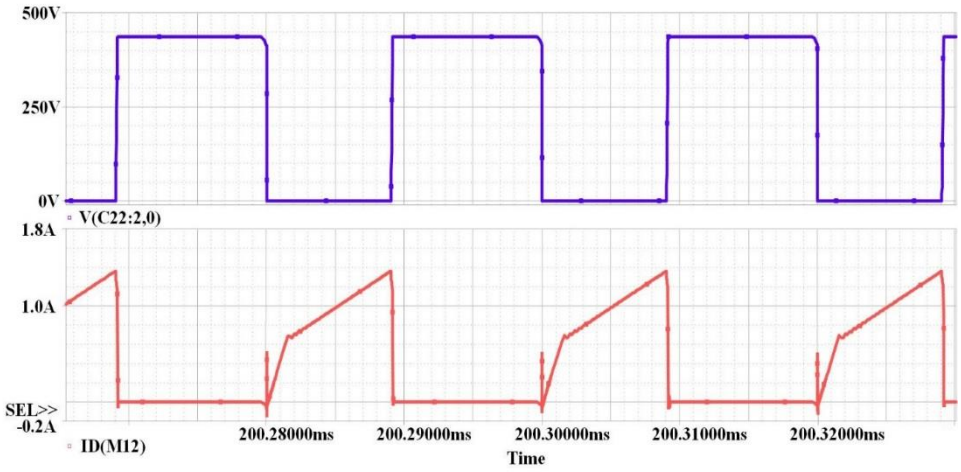

Figure 5. The voltage and current waveforms of the switch S_2

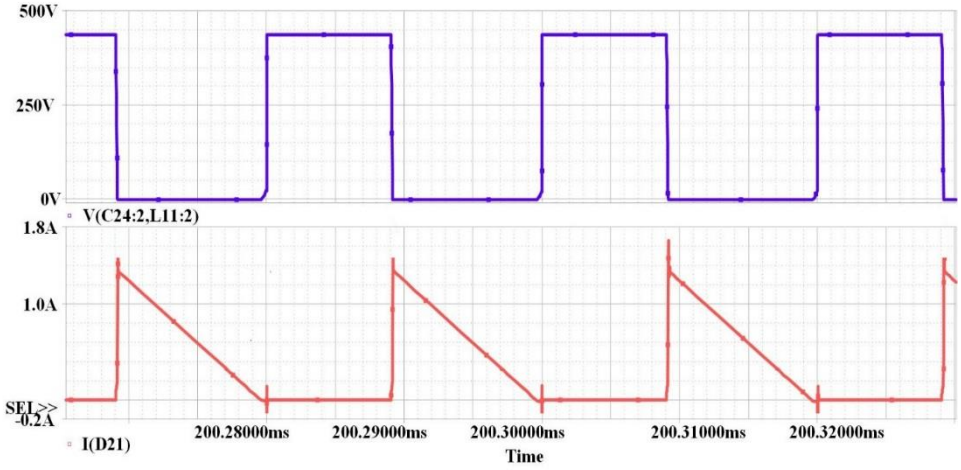

Figure 6. The voltage and current waveforms of the diode D_1

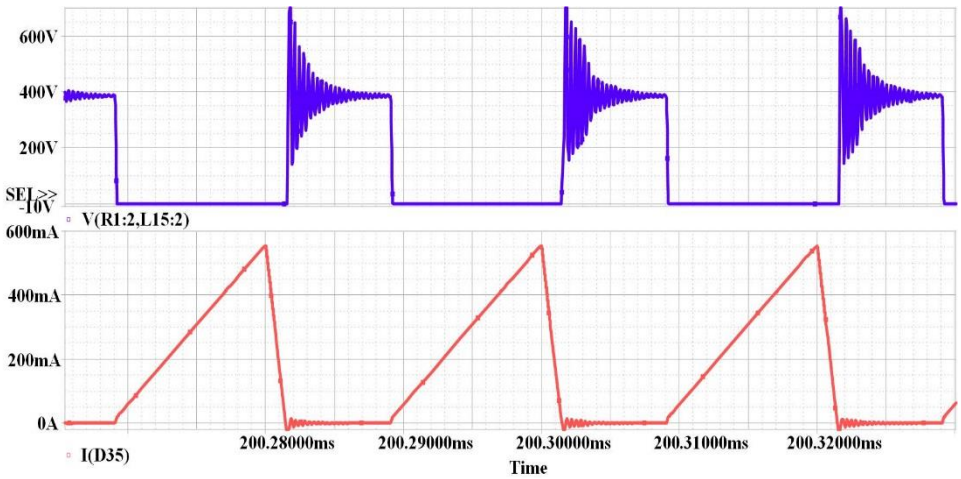

Figure 7. The voltage and current waveforms of the diode D_2

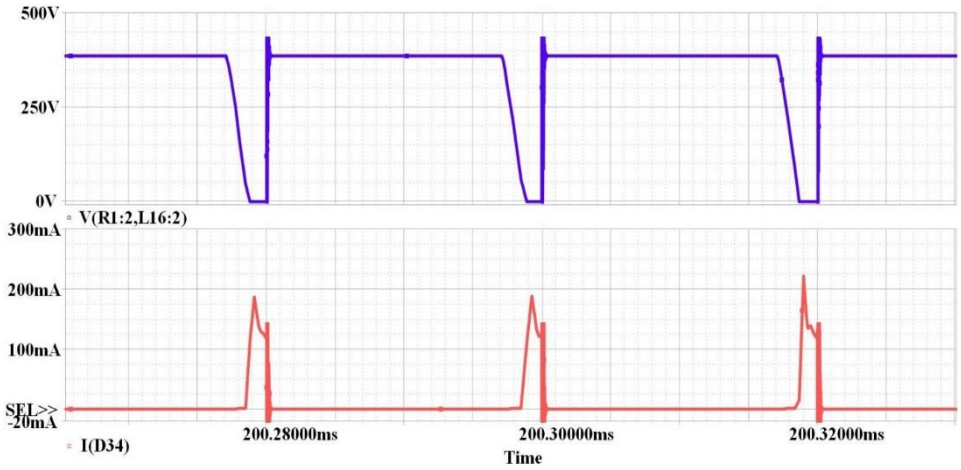

Figure 8. The voltage and current waveforms of the diode D_3

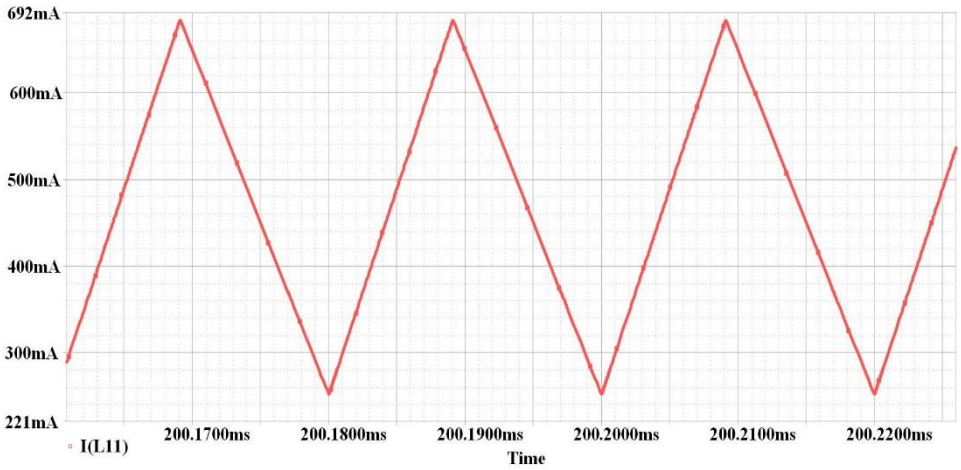

Figure 9. The current waveform of the inductor L_1

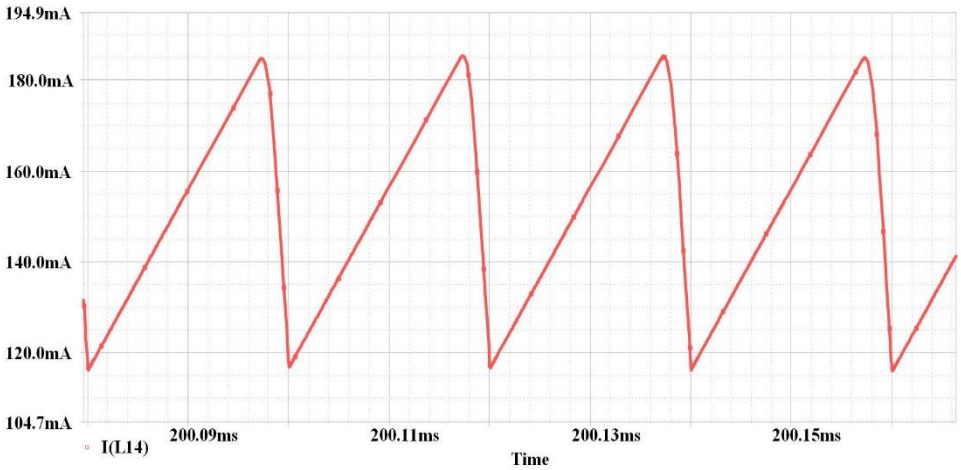

Figure 10. The current flowing through the inductor L_2

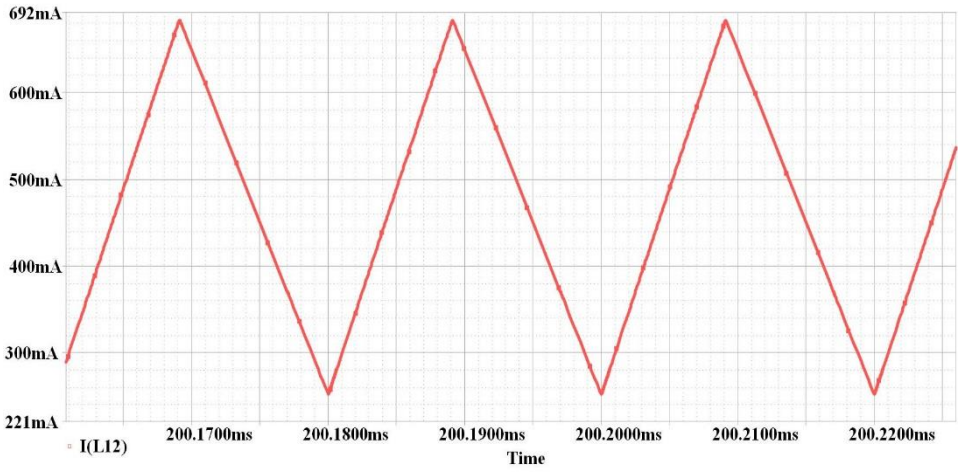

Figure 11. The current flowing through the inductor L_3

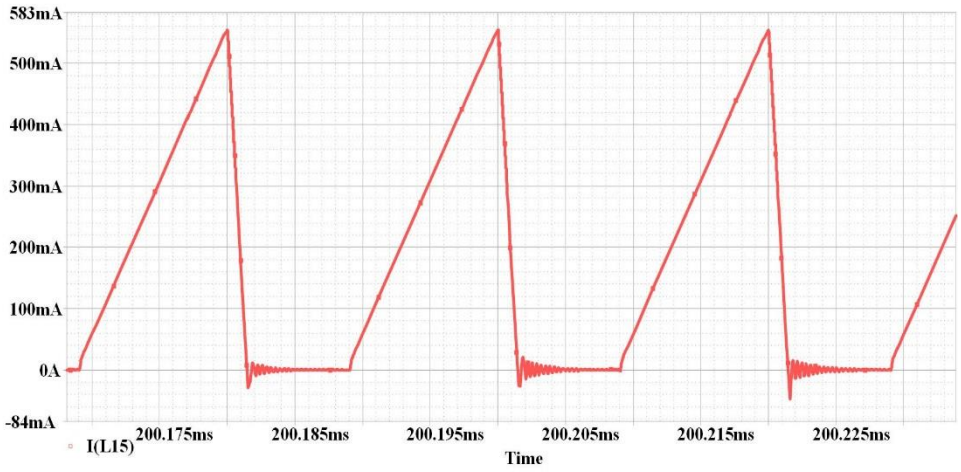

Figure 12. The current flowing through the inductor L_4

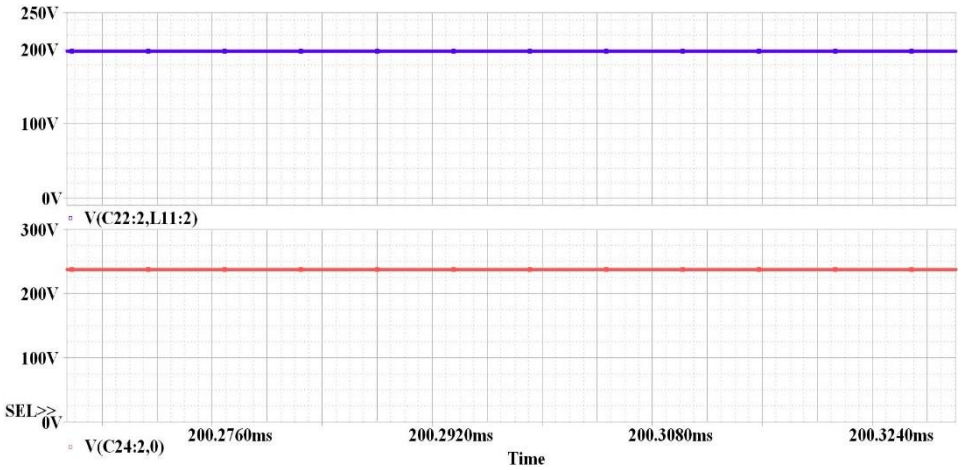

Figure 13. The voltage waveforms across the capacitors C_1 (red one) and C_2 (blue one)

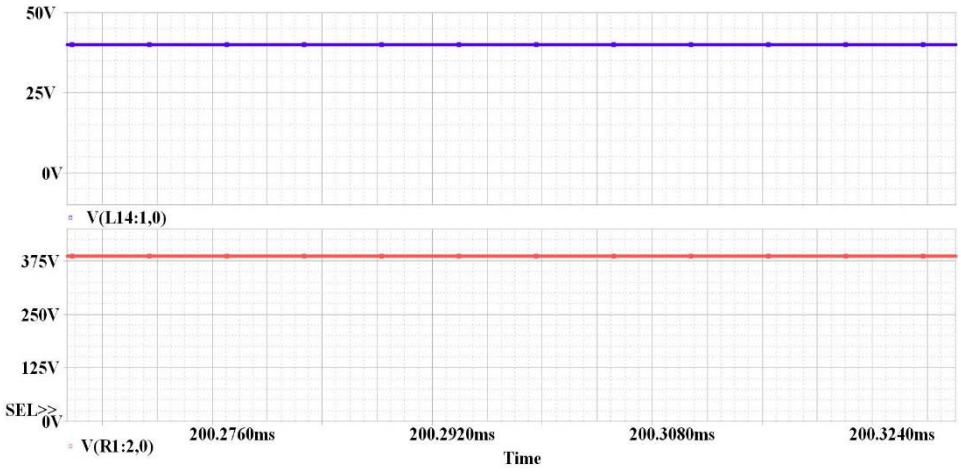

Figure 14. The input (blue one) and the output (red one) voltages waveforms of the proposed converter

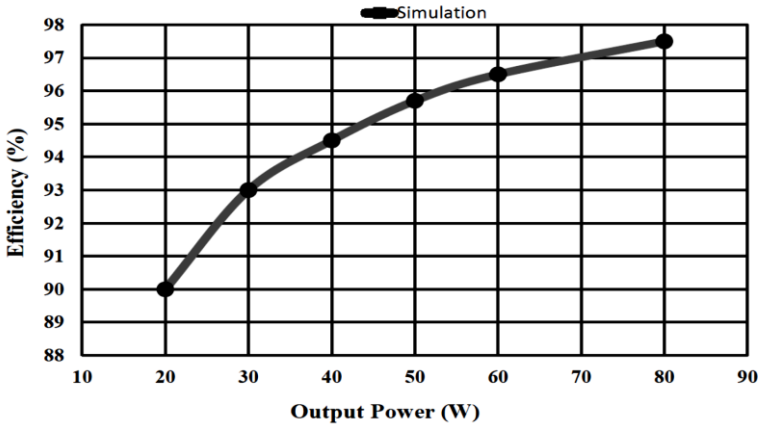

Figure 15. The characteristic curve of the proposed converter across various power levels

Figure 15 depicts the characteristic curve of the proposed converter across various power levels. This curve is derived by taking into account the parasitic elements of the proposed convertor. The efficiency is calculated at these different powers levels. Table 2 provides a comparative analysis of the proposed converter and other analogous Quasi-Z-Source DC–DC converters, focusing on parameters such as switching frequency and voltage gain. Power loss calculations for each component with important equations for the proposed converters are written in Table 3.

5. CONTROL OF PROPOSED CONVERTER

Figure 16 depicts the control circuit, which consists of four parts. The first part encompasses an output sampler circuit and feedback isolator, constructed using an optocoupler and TL431. The second part comprises an error amplifier and a PID compensator. The third part is the PWM controller, which generates gate-source voltage for switches by employing the SG3527 IC. The fourth section is the pulse delay circuit, which is utilized to adjust the produced signal by the former stage. Moreover, the performance of the control circuit during a sudden load change is shown in Figure 17.

6. CONCOLUSION

In this paper, a new structure is proposed, which is a parallel combination of a conventional boost converter and a Quasi-Z-Source converter. This circuit structure increases the voltage gain. Due to the current division between two parallel paths, the current stress on active and passive elements is reduced. On the other hand, the ohmic losses of the elements are reduced, and the efficiency of the converter is improved. One of the important features of the proposed converter is the common ground between the input and output. This eliminates the need for a gate driver with a floating ground. Additionally, less noise is generated in the converter's operation. Other advantages of this converter include a simple circuit structure, linear operation, simple control circuit, and PWM control. The presence of a large input filter inductor in the proposed converter ensures continuous input current, CCM operation, and suitable input current ripple. This converter is designed for 40V (input voltage) and 400V (output voltage) and then simulated using PSPICE software. The switching frequency is 50 kHz, and the nominal power of the converter is 80W. Mathematical relations and loss

analysis show that the efficiency of the converter at this power is about 96%. This converter has been compared with similar structures in various criteria. This comparison shows the suitable performance of the proposed converter compared to others.

Table 2: The comparison between the proposed converter with other QZ-source DC–DC converters

Ref.	Voltage gain	Switching frequency	Components	Voltage stress for input diode	Voltage stress for the main switch	Efficiency at 80 W	Soft switching	Volume
[30]	6.5	100 kHz	1 Switch 5 Diodes 2 Inductors 2 Capacitors	$\frac{D}{1-D}V_{in}$	$\frac{1+D}{1-D}V_{in}$	93%	No	Medium
[31]	7	50 kHz	1 Switch 3 Diodes 2 Inductors 4 Capacitors	$\frac{1}{1-2D}V_{in}$	$\frac{1}{1-2D}V_{in}$	63%	No	Small
[33]	8.5	40kHz	2 Switches 5 Diodes 2 Magnetic cores 5 Capacitors	****	***	93.8%	No	Large
[34]	7.5	50 kHz	2 Switches 3 Diodes 3 Inductors 4 Capacitors	$V_{D1}=\frac{2G-1}{5G}V_o$	$\frac{2G-1}{5G}V_o$	94.3%	No	Small
[35]	9.75	50 kHz	1 Switch 7 Diodes 2 Inductors 6 Capacitors	$V_{in}+V_{C2}$	$\frac{V_O}{3}$	94.8%	No	Large
[36]	5.5	50 kHz	1 Switch 6 Diodes 4 Inductors 5 Capacitors	$\frac{1}{1-4D+2D^2}V_{dc}$	$\frac{1}{1-4D+2D^2}V_{dc}$	94.5%	No	Large
[37]	10.7	100 kHz	2 Switch 5 Diodes 2 Inductors 5 Capacitors	$\frac{2}{1-D}$	$\frac{1}{1-D}$	98%	No	Small
Proposed	10	50 kHz	2 Switch 3 Diodes 5 Inductors 3 Capacitors	$V_{C1}-V_{C2}$	$V_{C1}+V_{C2}$	97.5%	Yes	Small
	*** $\begin{cases} V_{S1}=\frac{(G-G^2+G\sqrt{5G^2(6+4n)G+1})Vin}{(3G+2nG+1+\sqrt{5G^2(6+4n)G+1})} \\ V_{S2}=\frac{2G^2Vin}{(3G+2nG+1+\sqrt{5G^2(6+4n)G+1})} \end{cases}$ **** $V_{D1}=\frac{2G^2Vin}{(3G+2nG+1+\sqrt{5G^2(6+4n)G+1})}$							

Table 3. Power losses of the proposed converter

Type of Loss	Formula	Proposed Converter
Switching Loss in Switches	$(\frac{1}{2}V_{in}.I_O.(t_{on}+t_{off})+V_{in}.(I_O+I_{rr}).t_{rr}).F_{SW}$	$(0.5\times40\times0.\ 2\times(100+100)\times10^{-9}$ $+40\times(0.2+0.1)\times100\times10^{-9})\times50\times10^3$
Parasitic Capacitance Loss in Switches	$\frac{1}{2}.C_S.V_{DS}^2.F_{SW}$	$0.5\times20\times10^{-6}\times220^2\times50\times10^3$
Conduction Loss in Switches	$R_{ds}.F_{SW}.\int_0^T I_S^2.dt$	$0.18\times50\times10^3\times1\times10^{-5}$
Conduction Loss in the Diodes in Voltage Increasing Cell (D_1)	$I_{ave}.V_F$	0.75×0.5
Conduction Loss in the Output Diodes (D_2 and D_3)	$I_{ave}.V_F$	0.02×0.5
The Loss of Inductors	$P_{Loss}=P_{Core}+P_{Copper}$ $P_{Core}=K_1.F_{SW}.B^y.V_e$ $P_{Copper}=P_{DCR}+P_{ACR}=$ $I_{rms1}^2.DCR+I_{rms2}^2.ACR$	2.38
The Loss of Capacitors	$P_d=ESR+I_{ave}^2$	0.34
Total Losses	-	**P_{Loss}=3.2W**

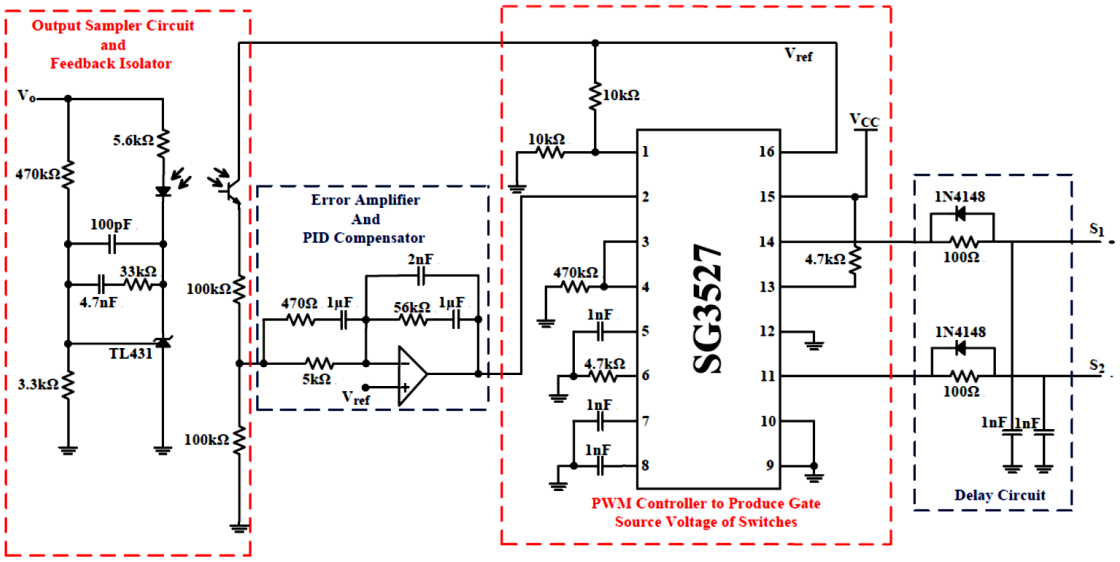

Figure 16. The control circuit

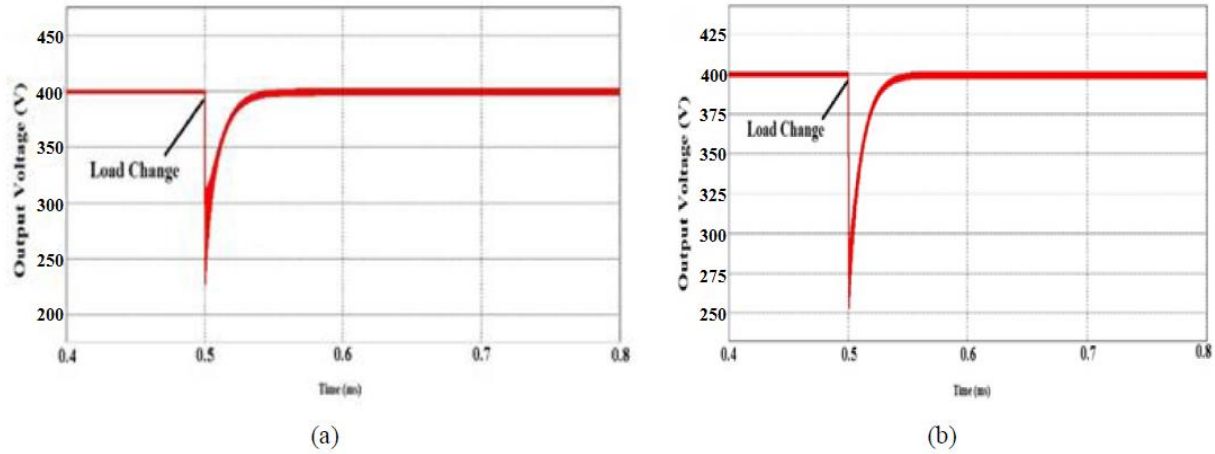

Figure 17. Performance of the control circuit during a sudden load change (a) 25% to 100% of rated load (b) 50% to 100% of rated load.

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