Bridgeless High Power Factor Buck-Converter Operating In Discontinuous Capacitor Voltage Mode

Nasrullah Mohammad Awni Khraim

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Bridgeless High Power Factor Buck-Converter
Operating in Discontinuous Capacitor Voltage Mode

By

Nasrullah Mohammad Awni Khraim

A thesis submitted to the College of Engineering in partial fulfillment of
the requirements for the degree of
Master of Science in Electrical Engineering

Master Program of Electrical Engineering
Department of Electrical Engineering
College of Engineering
United Arab Emirates University

January 2013
Thesis Title:
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Author
Nasrullah Mohammad Awni Khraim

A thesis submitted to the College of Engineering in partial fulfillment of the requirement for the degree of Master of Science in Electrical Engineering

Thesis Supervisor:
Dr. Abbas A. Fardoun

Thesis Examining Committee:
Prof. Malik E. Elbuluk
The University of Akron, Professor of Electrical & Computer Engineering
Dr. Hassan Hejase
UAE University, College of Engineering, Department of Electrical Engineering
Dr. Ala Al-Haj Hussein
UAE University, College of Engineering, Department of Electrical Engineering

Department of Electrical Engineering
College of Engineering
United Arab Emirates University
January 2013
List of Publications


3. Extended version of 1 is under preparation to be submitted to IEEE transactions on industry applications.
Abstract

High power factor AC-DC rectifiers have gained a lot of attention due to demanding international regulations. The International harmonics' standards, i.e. IEC 61000-3-2 and EN 61000-3-2 require low harmonic content of the main line current, or in other words, high power factor. Also, new market initiatives such as the 80 PLUS initiative, require high efficiency of the power supply. These standards specify the AC line current harmonics' limits depending on load and application.

In this research, a new converter, with high power factor and high efficiency, operating in discontinuous capacitor voltage mode (DCVM) – is investigated targeting personal computers (PC) and server applications. To the best of our knowledge, this is the first published bridgeless topology operating in DCVM.

To ensure high efficiency, the bridgeless rectifier topology is modified by eliminating two diodes and replacing them with two unidirectional switches. On the other hand, the DCVM has the advantages of no need for high frequency input filter, soft turn-off switching, low switch current stress and high efficiency at low loads.

A comparison between full bridge DCVM buck power factor correction (PFC) converter and the proposed topology is presented. The proposed topology found to have higher efficiency than that of the full bridge DCVM buck PFC converter, and less THD. Hence, the power factor has been significantly improved. The comparison is summarized and tabulated in chapter five.

Design procedure, simulation and measurements are in chapter five. Simulation results are presented to demonstrate the topology's performance. Orcad PSpice software has been used to simulate the proposed topology. Measurements are presented to verify the theoretical analysis and the simulation findings. The harmonics at the input current are also compared with the IEC 61000-3-2 harmonic standard values. A step by step design procedure for the converter has been developed at any operating point over universal line input voltage (90-265Vrms). Small signal analysis and bode plots for the proposed topology were developed for the line-to-output and control-to-output transfer functions.
Acknowledgements

I would like to thank Allah Almighty for blessing and giving me strength to accomplish this thesis. I also like to take the chance to thank everyone who helped and supported me in the accomplishment of this M.Sc. thesis document.

I would like to express my deep sense of gratitude to my supervisor Dr. Abbas Fardoun for all his guidance, comments and continuous support throughout the development of this thesis. He was available through the period of my research with his deep knowledge, rich experience, high cooperation, positive attitude, boundless energy and motivation. Also, I want to express my sincere gratitude and admiration to Dr. Esam Ismail for his support and valuable feedback.

I wish to thank the reviewers Drs. Malik Elbuluk, Hassan Hejase, Addy Wahyudie, Ala Al-Haj Hussein and Hassan Noura who, in addition to my supervisor, have read and commented on the manuscript. Their comments improved the readability and clarity of the thesis.

My unending appreciation goes to my father for his continuous encouragement, and all of my family members: especially my wife, my kids, my sisters, my brother and to all of the people who supported me and wished me the best of luck.

Last but not least, I would like to dedicate this work to the soul of my mother (May Allah the merciful forgives her).

Nasrullah Khraim
January 2013
Undertaking

I certify that research work titled "Bridgeless High Power Factor Buck-Converter Operating in Discontinuous Capacitor Voltage Mode" is my own work. The work has not been presented elsewhere for assessment. Where material has been used from other sources it has been properly acknowledged/referred.

Signature of Student
Nasrullah Mohammad Awni Khraim

January 2013
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Abbreviations

AC: Alternating Current

CCVM: Continuous Capacitor Voltage Mode

CoC: Code of Conduct

DC: Direct Current

DCVM: Discontinuous Capacitor Voltage Mode

DICM: Discontinuous Inductor Current Mode

EMI: Electromagnetic Interference

EPA: Environmental Protection Agency

IEC: International Electro-technical Commission

IGBT: Insulated Gate Bipolar Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PC: Personal Computer

PF: Power Factor

PFC: Power Factor Correction

RMS: Root Mean Square

THD: Total Harmonic Distortion

ESR: Equivalent Series Resistance
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</tr>
<tr>
<td>$K$</td>
<td>Kilo</td>
</tr>
<tr>
<td>$K_{Cr}$</td>
<td>Critical conduction parameter constant (unit-less)</td>
</tr>
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<td>$L_1, L_2$</td>
<td>Input inductors</td>
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<tr>
<td>$L_e$</td>
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<td>$P_o$</td>
<td>Output power</td>
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<td>$Q$</td>
<td>Switch</td>
</tr>
<tr>
<td>$R_{i-eff}$</td>
<td>Effective input resistance</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Resistive load</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Line cycle (Period)</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Switching cycle (Period)</td>
</tr>
<tr>
<td>$v_{ac}, v_{in}$</td>
<td>Sinusoidal input voltage</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input capacitor peak voltage</td>
</tr>
<tr>
<td>$V_{df}$</td>
<td>Diode forward drop voltage</td>
</tr>
<tr>
<td>$V_{in}, V_I$</td>
<td>Input voltage (Peak value)</td>
</tr>
<tr>
<td>$\hat{v}_L(t)$</td>
<td>Inductor small-signal voltage</td>
</tr>
<tr>
<td>$\langle v_L(t) \rangle_{T_S}$</td>
<td>Inductor low-frequency averaged voltage</td>
</tr>
<tr>
<td>$V_o$</td>
<td>Output voltage</td>
</tr>
<tr>
<td>$Z_{eq}$</td>
<td>Equivalent impedance</td>
</tr>
<tr>
<td>$Z_L$</td>
<td>AC line impedance</td>
</tr>
</tbody>
</table>
Nomenclature

\( \eta \) Efficiency
\( \mu \) Micro
\( \theta_i \) Current phase angle
\( \Delta I_{in} \) Input current ripple
\( \omega_L \) Line angular frequency
\( \varphi_r \) Voltage phase angle
\( \Delta V_o \) Output voltage ripple
\( C_1, C_2 \) Input capacitors
\( C_o \) Output capacitor
\( D \) Duty cycle
\( D_I \) Normalized discharging time
\( D_{r}, D_p \) Return diodes
\( D_o \) Output diode
\( E_{in} \) Input energy over half-line cycle
\( E_o \) Output energy over half-line cycle
\( f_L \) Line frequency
\( f_S \) Switching frequency
\( G_{vd}(S) \) Control-to-output transfer function
\( G_{vg}(S) \) Line-to-output transfer function
\( I_0 \) Input Current "DC component"
\( I_i \) Input Current "fundamental component"
\( I_2, I_o \) Output current
\( I_{Bridge} \) Bridge rectifier current
\( I_{Bridgeless} \) Bridgeless rectifier current
\( I_n \) Input Current "n\textsuperscript{th} component"
\( I_Q \) Switch current
Due to the extraordinary increase in the use of such non-linear loads, international standards such as IEC 61000-3-2 Class D and EN 61000-3-2 [1, 2, 6, 7] were introduced to limit the harmonics induced by non-linear loads in the AC system. These standards require that the harmonics contents of the non-linear equipment connected to mains stay below certain limits. High quality rectifiers shall comply with the harmonics' international standard for electronic equipment, i.e. personal computers, PC-monitors and television receivers.

1.2 International Line Current Harmonics Standards

Power electronic devices used in personal computers, PC monitors, TV receivers, etc. are provided with rectifiers to convert the AC to DC. Rectifiers generate current harmonics and pollute the power quality, and result in a low power factor. Therefore, international standards, i.e. IEC 61000-3-2 and EN 61000-3-2 were introduced to limit the harmonics induced by non-linear loads in the AC system and to minimize power pollution [1-2].

1.2.1 Classification and Limits

There are four different classes in the EN 61000-3-2 and in the IEC 61000-3-2 that have different limit values:

Class A: Balanced 3-phase equipment,

Household appliances excluding equipment identified as class D,

Tools, excluding portable tools,

Dimmers for incandescent lamps,

Audio equipment,

Everything else that is not classified as B, C or D.

Class B: Portable tools,

Arc welding equipment which is not professional equipment

Class C: Lighting equipment.
Chapter 1

Introduction

1.1 Background

The continuous development in the electronic devices technology has some drawbacks such as distorting the AC line current with harmonic contents. Power electronic devices such as AC/DC converters are nonlinear loads that are widely used in personal computers, PC monitors, television receivers, printers, laptops and cellular phones that generate harmonics in the AC line current [1]. Fig. 1.1 shows some of the linear and non-linear sources of distortion and harmonic currents, which are fed from AC supply with a line impedance $Z_L$. The resultant AC system current will be distorted. This non-sinusoidal current has a lot of harmonics that negatively affect on the linear loads, such as home appliances, refrigerators, washing machines and air conditioners. Hence, linear loads suffer from poor performance, greater thermal losses, lower power factor and life degradation. Also, the system voltage waveforms will be deformed and certain power system protection elements may malfunction [1-5].

Fig. 1.1: Sources of distortion and harmonic currents.
need less energy to supply the computer system with the same power. All five standards are defined in Table 2 [9].

Table 2: 80 PLUS initiative standards [9].

<table>
<thead>
<tr>
<th>80 PLUS Test Type</th>
<th>115V Internal Non-Redundant</th>
<th>230V Internal Redundant</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fraction of Rated Load</td>
<td></td>
</tr>
<tr>
<td></td>
<td>20%</td>
<td>50%</td>
</tr>
<tr>
<td>80 PLUS Standard</td>
<td>80%</td>
<td>80%</td>
</tr>
<tr>
<td>80 PLUS Bronze</td>
<td>82%</td>
<td>85%</td>
</tr>
<tr>
<td>80 PLUS Silver</td>
<td>85%</td>
<td>88%</td>
</tr>
<tr>
<td>80 PLUS Gold</td>
<td>87%</td>
<td>90%</td>
</tr>
<tr>
<td>80 PLUS Platinum</td>
<td>90%</td>
<td>92%</td>
</tr>
</tbody>
</table>

The initiative was involved in the adoption by the environmental protection agency (EPA) of the Energy Star 4.0 computer specification, as well as in the European Code of Conduct (CoC) document [10]. Energy Star rated computers must now include the 80 PLUS power supplies (or equivalent). 80 PLUS succeeded also in involving two of the largest computer equipment manufacturers, Dell and HP. These two companies claimed rebates for 10,276 units shipped in December of 2007 alone. [11]

In order to allow consumers to know which power supplies are most efficient, manufacturers are using stickers with 80 PLUS logo colored as per the efficiency level certification. As shown in Table 2 and Fig. 1.2.

Fig. 1.2: 80 PLUS categorized stickers [9]
Class D: Personal computers and personal computer monitors, radio, or TV receivers.

Note: Equipment must have an input power level as follows: \( 75 \text{W} \leq P \leq 600 \text{W} \)

The topic "Operation of rectifiers with high power factor and low line current distortion" has become a very active area of research to achieve the international standards, i.e. IEC 61000-3-2 Class D requirements.

Table 1 shows the maximum permissible harmonic current levels and a guideline to the EN 61000-3-2 standard regarding reducing harmonic current emissions. [1-2]

Table 1: Limits of maximum permissible harmonic current levels of class D equipment (EN 61000-3-2 Standard) [2].

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>Maximum permissible harmonic current per watt</th>
<th>Maximum permissible harmonic current</th>
<th>Normalized Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>mA/W</td>
<td>A</td>
<td>(%)</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>3.69</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>3.4</td>
<td>2.3</td>
<td>0.62</td>
</tr>
<tr>
<td>5</td>
<td>1.9</td>
<td>1.14</td>
<td>0.31</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0.77</td>
<td>0.21</td>
</tr>
<tr>
<td>9</td>
<td>0.5</td>
<td>0.4</td>
<td>0.11</td>
</tr>
<tr>
<td>11</td>
<td>0.35</td>
<td>0.33</td>
<td>0.09</td>
</tr>
<tr>
<td>( 13 \leq n \leq 39 ) (Odd harmonics only)</td>
<td>( 3.85/n )</td>
<td>( 0.23 * (8/n) )</td>
<td></td>
</tr>
</tbody>
</table>

1.3 80 PLUS and Other Initiatives

A new market initiative, the 80 PLUS Initiative, calls for high efficiency converters. Saving energy is already a critical task in many parts of the world and started to become an issue. Computer systems are demanding more power than before which can be credited to factors like faster video cards or processors, larger hard drives and other components that raise the power consumption of a computer [8].

80 Plus initiative now certifies power supply units with energy efficiency of 80% or more and true power factor of 0.9 and more. This means that these power supply units
Disortion Factor = \left( \frac{1}{\sqrt{1 + (THD)^2}} \right) \quad (1.4)

Fig. 1.3: Distortion factor vs. total harmonic distortion [3].

1.5 Objectives and Thesis Outline

The main objective of this research is to design and analyze a bridgeless buck topology converter with High Power Factor & High Efficiency operating at universal-line voltage ranges (90-265Vrms). The objective was divided into a number of tasks as shown below:

a) Analyze and review published literature for related application.

b) Identify a new topology to improve power factor and efficiency. And verifying the principle of operation to achieve the expectation of higher efficiency and higher power factor.

c) Compare new topology to existing published ones.

d) Identify operating point based on the application of interest.

e) Verify equations using simulation “using Orcad PSpice software”.

f) Compare the harmonics of the AC line current with IEC 61000-3-2 standard.
1.4 Harmonics of the Input Voltage

Harmonics of line current are expressed as a function of power factor. Power factor is a product of two terms. The first term is the distortion factor, which is the ratio of the RMS value of the fundamental component to the total RMS value of the current. [3]

\[
\text{Distortion Factor} = \frac{I_1}{\sqrt{\frac{1}{2} I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}}
\]  
(1.1)

Where \( I_1 \) is the RMS value of the fundamental component, \( I_0 \) is the DC component and \( I_n \) is the \( n \)th component of the input current.

The other term is the displacement factor, which occurs due to load dynamics and reactive components, \( \cos(\phi_n - \theta_I) \) term, assuming an ideal sinusoidal input. [3]

\[
\text{Power Factor} = \frac{I_1}{\sqrt{\frac{1}{2} I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \left( \cos(\phi_n - \theta_I) \right)
\]  
(1.2)

\( (\text{Distortion Factor})(\text{Displacement Factor}) \)

Where \( \phi_n \) and \( \theta_I \) are the phase angles of the AC input voltage and the AC input current respectively. As a rule of thumb, low total harmonic distortion (THD) for a pure sinusoidal current means a high power factor. Fig. 1.3 shows the relation between the distortion factor versus THD [3].

THD is known as the ratio of the RMS value of the waveform but excluding the fundamental, to the RMS fundamental magnitude. When there is no DC, this can be written as shown in eq. (1.3),

\[
\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}
\]  
(1.3)

The relation between THD and the distortion factor is shown in the comparison of eqs. (1.1) and (1.3), with DC component being zero \( I_0 = 0 \):
Chapter 2

Literature Review

Most of the electronic devices e.g. computers, telecom, and networking equipment at different load levels require DC power which are obtained using AC-to-DC rectifiers [10]. Since the output voltage of the passive rectifiers contains high amount of harmonics low pass filters are used at the load side of the rectifier to minimize the voltage ripple. However, the power density is reduced. PFC rectifiers address this issue.

In this chapter, different types of passive and active rectifier topologies are presented. In addition, a literature review for full bridge and bridgeless topologies is discussed. Comparison between DCVM and DICM is shown.

2.1 Passive Rectifiers

Passive PFC circuits can achieve high power factor without losses and with high efficiency; however, these circuits put more stress on the semiconductor components. Moreover, the volume of the rectification circuitry is greater, in other words, the power density is reduced so the system cost increases [6, 21-26].

2.1.1 Passive Full Bridge Rectifier Without Filter

Full bridge rectifier or conventional bridge rectifier, shown in Fig. 2.1, is the most basic rectifier used to compensate for the line current harmonics. The diode bridge connects the capacitor to the AC source when the voltage is near the peak, resulting in an abridged sinusoidal shaped input line current waveform for about 1 to 2 ms every half cycle [23] as shown in Fig. 2.2. To minimize the output current ripple, the capacitor $C_o$ is large enough.
g) Compare the efficiency of the proposed topology with a full bridge buck PFC converter operating in DCVM [15], at different universal AC line voltages.

h) Set a design procedure for selecting the proposed topology components.

i) Small signal model for the proposed topology.

j) Test the topology experimentally in order to verify the theoretical analysis and the PSpice simulation results.

1.6 Applications of the Proposed Topology

The proposed topology is a high power factor and a high efficiency converter that can operate at universal-line voltage ranges (90-265 Vrms). Since it is targeting the international harmonics' standards, i.e. IEC 61000-3-2 and EN 61000-3-2 which require the harmonic contents of the equipment connected to the mains, be under a specified limit. The applications of this proposed topology can be:

- Power supply units for servers, laptops and PC applications with energy efficiency complying with 80 PLUS initiative.
- TV monitors, TV receivers.
- All low DC voltage applications that require high power factor & high efficiency power supplies with minimum THD.
- Typical loads between 75W and 600W. [1, 2, 12-14]
As a result, the power factor and THD are slightly improved, but still not satisfying IEC standards. One of the methods used to compensate for the drawbacks of the passive approach is to use active PFC rectifiers.

### 2.2 Active Rectifiers

Active PFC circuits achieve unity power factor in low voltage applications. However, the conduction and switching losses are considered to be high in heavy loads [27]. They are used to enhance the overall performance of the rectifier circuit in comparison to the passive approach [28-38].
The distorted nature of the input AC line current in the full bridge rectifiers is creating potential problems for the AC voltage supply, which affects the power factor dramatically. The passive full bridge rectifiers (without filters) do not satisfy the harmonics’ standards IEC 61000-3-2 (Class D) due to the low power factor and low efficiency as well. Therefore, researchers work to improve this factor.

### 2.1.2 Passive Full Bridge Rectifier With Filter

In order to improve the harmonic content of the line current of the passive full bridge rectifier; Full bridge rectifier with a filter is used. An inductor in series with the voltage source is added, as shown in Fig. 2.3. The input current and the input voltage are shown in Fig. 2.4.
DCVM can be achieved in topologies with two inductors that emulate positive and negative current sources needed to charge and discharge the capacitor. To obtain DCVM, the inductors must have large enough inductances so that the current through them can be considered constant during one switching cycle, and the input capacitor must have low enough capacitance so it can be discharged before the beginning of a new switching cycle [38].

Fig. 2.6 shows a full bridge Čuk convertor operating at DCVM and DICM.

Fig. 2.6: Full bridge Čuk convertor operating at DCVM and DICM [6, 20].

However, a lot of work has been performed on DCVM with full bridge rectifier circuits which improved the power factor over the DICM bridge PFC circuits in some applications and in certain conditions, still the efficiency did not improve [16-28].

Full bridge rectifiers have low efficiency comparing to the bridgeless rectifiers. There are four diodes conducting in the full bridge rectifiers, hence, the losses are higher considering the forward voltage drop $V_{df}$ of the diodes. The current flowing in each of the bridge diodes is calculated by,

$$I_{Bridge} = \frac{P_{out}}{\eta V_{in, rms}} \tag{2.1}$$

The power dissipated (losses) in the bridge rectifier diodes is expressed as follows,

$$P_{Bridge, losses} = 4 V_{df} I_{Bridge} = 4 V_{df} \frac{P_{out}}{\eta V_{in, peak}} \tag{2.2}$$

Assuming that a universal input voltage $v_{in} = 120$ Vrms, and the diode forward voltage drop $V_{df} = 1$ V. Then, the power dissipation in the bridge rectifier is presented as,
2.2.1 Full Bridge PFC Rectifier

Full Bridge rectifiers have a relatively low efficiency due to the number of silicon components in the current path of each stage [6, 21-26]. For example, the full bridge boost rectifier shown in Fig. 2.5 where the current flows through three power semiconductor switches during each switching cycle. When the switch $Q$ is turned on, the current flows through two rectifier bridge diodes $D_1$ and $D_4$ and the power switch $Q$. While it flows through two rectifier bridge diodes $D_2$ and $D_3$ and the output diode $D_o$ during the switch $Q$ is turned off. The forward voltage drop across the bridge diode causes significant conduction losses, resulting in more severe thermal stresses.

![Fig. 2.5: Full bridge boost PFC topology [4].](image)

2.2.2 Full Bridge PFC Rectifier with DICM and DCVM Operations

In efforts of improving the power factor, further studies have been conducted on the discontinuous inductor current mode (DICM) and discontinuous capacitor voltage mode (DCVM) operations with full bridge PFC circuits for low power applications. The power factor was improved. However, efficiency was still lower than required. [26, 39-40]

DICM occurs when the current through the inductor $L$ is completely discharged to zero before the beginning of a new switching cycle. While DCVM occurs when the capacitor $C$ is completely discharged to zero before the beginning of a new switching cycle. As a result, the voltage across the capacitor in DCVM varies in a similar way as the current through an inductor in DICM. Inherent PFC properties are obtained in DCVM [3]. DCVM can be considered as dual of DICM [38].
2.2.3 Bridgeless PFC Rectifier

In a bridgeless rectifier, the number of diodes conducting at any instant of time is reduced. It is characterized by high efficiency due to the reduced forward and backward drop voltage and line losses through the components, in addition to the high power density [9, 16, 28, 41].

The bridgeless PFC circuit improves efficiency, reduces costs, and enables simplicity and high performance. As a result, it has gained popularity as a high-efficiency AC-DC rectifier compared to the full bridge PFC rectifier [4, 16, 18, 28].

Fig. 2.9 to Fig. 2.11 show, respectively, the topologies of the bridgeless boost PFC, bridgeless buck PFC, and bridgeless Čuk PFC converters.

![Bridgeless boost PFC converter topology](image1)

Fig. 2.9: Bridgeless boost PFC converter topology [28, 31].

![Bridgeless buck PFC converter topology](image2)

Fig. 2.10: Bridgeless buck PFC converter topology [29].
\[ P_{\text{Bridge losses}} = 4 \frac{V_d f}{V_{\text{Bridge}}} = 4 \left(1 - \frac{P_{\text{out}}}{\eta (120 \sqrt{2})} \right) = (2.35 \%) \frac{P_{\text{out}}}{P_{\text{in}}} = (2.35 \%) P_{\text{in}} \quad (2.3) \]

As a conclusion, since the bridgeless rectifiers contain two diodes only, then their power loss is almost half of that of the full bridge rectifiers.

A full bridge buck PFC converter operating in DCVM [15] is shown in Fig. 2.7. The switch operates all over the line cycle, which means that the switch current stress will be more than that of the proposed bridgeless DCVM topology.

![Fig. 2.7: Full bridge buck PFC converter operating in DCVM [15].](image)

While the modified Sheppard-Taylor converter topology [18], shown in Fig. 2.8, consists of a relatively big number of components. Which implies that the efficiency will not be high enough. Moreover, the voltage stresses across the capacitor C and the switches are considered to be high. Also, the current stress through the switch is very high.

![Fig. 2.8: Modified Sheppard-Taylor converter topology [18]](image)
2.4 Comparison of DCVM and DICM

A comparison between DCVM and DICM is illustrated in Table 3 [6, 15-17, 20, 25, 28, 29, 35].

<table>
<thead>
<tr>
<th>Voltage Stress</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>High at the active switch and output diode, which affecting the efficiency.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current Stress</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>High current stress and heavy conduction loss.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AC line current ripple</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low. Provides continuous input current. As a result, no high frequency input filter is required.</td>
<td>Large. Provides discontinuous input current, with tougher requirements for the input filters, leading to lowering the power factor.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Switching characteristic</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft turn-on</td>
<td>Soft turn-off</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Switches</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>IGBT</td>
<td>IGBT or MOSFET</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Loading characteristic</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>The higher the load &quot;smaller load resistance&quot;, the deeper the converter operates in DCVM, and the higher in power factor.</td>
<td>The lighter the load &quot;higher load resistance&quot;, the higher in power factor.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Applications</th>
<th>DCVM</th>
<th>DICM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low voltage, high current.</td>
<td>Low current, high voltage.</td>
<td></td>
</tr>
</tbody>
</table>
Fig. 2.11: Bridgeless Ćuk PFC converter topology [41].

Up to this stage, no studies have been conducted on the bridgeless PFC converters operating in DCVM. In the proposed topology, a bridgeless PFC circuit is used with DCVM. The DCVM improved the power factor, and the bridgeless circuit enhanced the efficiency. Suitable LC filters are added to the input of a buck converter which forced the converter into DCVM operation. As a result, the AC line current contains less harmonics and lower THD [15-19].

2.3 DCVM Advantages

DCVM and DICM have inherent power factor correction properties. However, DCVM has some advantages over DICM, besides the fact that DCVM is characterized by a high power factor and low THD in the input current:

- The active switches $Q_1$ and $Q_2$ are turned-off at zero-voltage. As a result, the losses due to the turn-off switching are considerably reduced [16, 28].
- The output diode $D_o$ is turned-on at zero-voltage. Therefore, the losses due to turning-on the output diode are significantly decreased [6].
- No high frequency input filter is required due to the continuous input current that can be obtained with converters operating in DCVM [28].
- Low switching current stresses, hence, the conduction loss is minimized [6, 12, 28].
The topology has a common output stage with an LC filter similar to buck converter. The new bridgeless DCVM circuit converts the input AC to a stepped-down DC in one stage, and reduces the stage of converting AC to DC.

![Fig. 3.2: Block diagram for the bridgeless DCVM buck-converter.](image)

For some applications, additional DC-DC stage is required as shown in Fig. 3.3.

![Fig. 3.3: Block diagram for the full bridge PFC.](image)

### 3.2 Symmetry of Operation

The topology operates in symmetry during the positive and negative half-line cycles. During positive half-line cycle, the components $L_1-C_1-Q_1-L_o-D_o$ are active through diode $D_p$, which connects the input AC source to the output. As shown in Fig. 3.4

![Fig. 3.4: Proposed topology during the positive half-cycle.](image)

During the negative half-line cycle, the components $L_2-C_2-Q_2-L_o-D_o$ are active through diode $D_n$ which connects the input AC source to the output, as shown in Fig. 3.5.
Chapter 3

Proposed Topology Analysis

In this chapter, the proposed buck converter topology operating in DCVM is analyzed. Closed form equations of the gain as a function of the control signal, components’ stresses, small signal model and converter constraints are derived.

3.1 Proposed Topology

The DCVM bridgeless topology is shown in Fig. 3.1.

![Diagram of bridgeless high power factor buck-converter](image)

Fig. 3.1: Bridgeless high power factor buck-converter operating in DCVM.

The bridgeless rectifier, shown in Fig. 3.1, utilizes two power switches ($Q_1$ and $Q_2$). These power switches can be driven by the same control signal, which significantly simplifies the control and gating circuitry. Compared to the full bridge DCVM buck topology [16, 17], the structure of the topology utilizes one additional inductor and one capacitor. The additional components are added to improve the PFC step down capability in both positive and negative paths of the line cycle. The additional components are often described as a disadvantage in terms of size and cost. However, a better thermal performance is achieved with the two inductors compared to a single inductor. In addition, the continuous current is achieved without additional input filter.
3.4.1 First Stage

This stage starts when the switch $Q_1$ is turned on when $(0 \leq t \leq D_1T_s)$. The switch current $i_{Q1}$ is equal to the output inductor $L_o$ current $i_2$. In this stage, the input capacitor $C_1$ discharges at a rate of the difference between the input inductor’s current $i_1$ and the output inductor’s current $i_2$. During this stage the diode $D_o$ is reverse-biased by the voltage across the capacitor $C_1$. This stage ends when the current through the input capacitor $C_1$ decreases to zero at $t = D_1T_s$.

The switch current can be expressed as:

$$i_{Q1} = i_{Lo} = I_2 \quad (3.1)$$

The input capacitor charging current can be expressed as:

$$i_{C1} = i_1 - i_{Q1} = I_1 - I_2 \quad (3.2)$$

For a buck converter $I_2 > I_1$, hence, the rate of change of the input capacitor voltage is negative. This stage ends when the voltage across the input capacitor decreases until it reaches zero, as shown in Fig. 3.7.

$$\frac{dv_{C1}}{dt} = \frac{I_1 - I_2}{C_1} \quad (3.3)$$

From Fig. 3.7, the following equations can be extracted,

$$\frac{dv_{C1}}{dt} = \frac{I_1 - I_2}{C_1}$$

Fig. 3.6: Equivalent circuit during first stage, $(0 \leq t \leq D_1T_s)$.  

Fig. 3.7: Voltage across the input capacitor $C_1$ during switching-cycle with DCVM.
3.3 Assumptions of Analysis
The assumptions considered in the analysis of the proposed topology are:

1. All components used are assumed to be lossless.
2. The converter is operating at a steady-state condition.
3. The input voltage is assumed to be purely sinusoidal.
4. The inductors $L_1$ and $L_2$ are assumed to be large enough such that the current through them can be considered constant over one switching cycle. The current that flows through the output inductor $L_o$ is considered to be constant not only during one switching cycle but also during one half cycle of the line frequency.
5. The output capacitor $C_o$ is assumed to be large enough such that the output voltage $V_o$ can be considered constant, not only during one switching cycle but also during one half cycle of the line frequency.
6. The input capacitors $C_1$ and $C_2$ are assumed to have low enough capacitance values to operate in DCVM over a switching cycle.

3.4 Principles of Operation
The converter is analyzed only during the positive half-line cycle because of the symmetry of operation during both positive and negative half line cycles. The operation in DCVM during the positive half-line cycle is divided into three distinct operating stages during one switching period $T_s$ as follows:
The analytical equations explaining this interval are presented by:

\[ v_{c1}(t) = 0 \]  
(3.10)

\[ i_{q1}(t) = i_{q2}(t) = I_1 \]  
(3.11)

The length of this interval is expressed as:

\[ \Delta t_2 = D_2 T_s = (D - D_1) T_s \]  
(3.12)

This stage ends with the switch \( Q_1 \) turned off at the time \( DT_s \). The output diode \( D_o \) is turned-on at zero-voltage. Therefore, the switching losses of turning-on the output diode are zero.

### 3.4.3 Third Stage

In this stage \((DT_s \leq t \leq T_s)\), switch \( Q_1 \) is turned off, as shown in Fig. 3.9. The input capacitor \( C_1 \) is charged by the input current \( i_I \). Hence, the input capacitor voltage \( v_{c1} \) increases linearly and reaches to the maximum value at \( V_{CM} \) at the end of the switching cycle \( T_s \).

![Fig. 3.9: Equivalent circuit during third stage, \((DT_s \leq t \leq T_s)\).](image)

The input capacitor is charged by the input current:

\[ i_{c1} = I_1 \]  
(3.13)

From Fig. 3.9, the following equations are extracted,

The slope of the rate of change of the input capacitor voltage is positive, and the capacitor voltage increases in this period until it reaches its maximum value at \( V_{CM} \), as shown in Fig. 3.7.
where $V_2 < V_1$ and $I_1 < I_2$. The analytical equations explaining this interval are presented by:

$$v_{C1}(t) = \frac{(I_1 - I_2)}{C_1} t + V_{CM}$$  \hspace{1cm} (3.4)

$$i_{Q1}(t) = i_{Q2}(t) = I_2$$  \hspace{1cm} (3.5)

The length of this interval can be derived as:

$$\Delta t_1 = D_1 T_s = \frac{C_1 V_{CM}}{I_2 - I_1}$$  \hspace{1cm} (3.6)

The peak voltage of the input capacitor $V_{CM}$ is calculated by:

$$V_{CM} = \frac{I_2 - I_1}{C_1} D_1 T_s$$  \hspace{1cm} (3.7)

### 3.4.2 Second Stage

In this stage, switch $Q_1$ is still turned on, as shown in Fig. 3.8, and $D_1 T_s \leq t \leq D T_s$.

As the input capacitor voltage is completely discharged by the end of the previous stage ($v_{C1} = 0$), the switch current $i_{Q1}$ is equal to the input current $i_I$. The output diode $D_o$ is forward-biased with a current equals to the difference between input inductor current $i_I$ and output current $I_o$.

![Equivalent circuit during second stage](image)

Fig. 3.8: Equivalent circuit during second stage, $(D_1 T_s \leq t \leq DT_s)$.

The input capacitor is completely discharged:

$$i_{C1} = 0$$  \hspace{1cm} (3.8)

The switch current can be expressed as:

$$i_I = i_{Q1} = I_2$$  \hspace{1cm} (3.9)

From the equivalent circuit shown in Fig. 3.8, the following equations can be extracted,
3.5 Input Capacitor Voltage

The voltage of the input capacitor $v_C(t)$ can be defined by substituting eqs. (3.4), (3.10), (3.15) and (3.18) as follows:

$$v_C(t) = \begin{cases} 
\frac{1}{C_1} \left[ I_1 (1-D)T_s + (I_1 - I_2)t \right], & 0 \leq t \leq D_1T_s \\
0, & D_1T_s \leq t \leq DT_T_s \\
\frac{I_1}{C_1} (t - DT_T_s), & DT_T_s \leq t \leq T_s 
\end{cases}$$

(3.20)
\[
\frac{d v_{c_1}}{dt} = \frac{I_1}{C_1}
\]  
(3.14)

The analytical equations explaining this interval are presented by:

\[ v_{c_1}(t) = \frac{I_1}{C_1} (t - DT) \]  
(3.15)

\[ i_{q_1}(t) = i_{q_2}(t) = 0 \]  
(3.16)

The length of this interval is expressed by:

\[ \Delta t_3 = D_3 T_s = D'T_s \]  
(3.17)

The peak voltage of the input capacitor \( V_{CM} \) is reached at the end of the cycle \( T_s \).

\[ V_{CM} = \frac{I_1}{C_1} D'T_s \]  
(3.18)

The derivation is shown in Appendix C.1

Equalizing eq. (3.7) and eq. (3.18) yields to:

\[ D_1 = \frac{I_1}{I_2 - I_1} D' \]  
(3.19)

The active switches \( Q_1 \) and \( Q_2 \) are turned-off softly at zero-voltage. Hence, the turn-off switching losses are considerably equal to zero. Also, EMI is reduced due to soft turning off.

Theoretical waveforms over one switching cycle \( T_s \) during the positive half-cycle of the input voltage is shown in Fig. 3.10.

These waveforms represent the behavior of topology components during the operation. The voltage waveforms across the output diode \( v_{do} \) and the switch \( v_{qi} \) show expected voltage stress on these components, which are useful in the design stage in selecting the components. Also, these waveforms illustrate the switch zero-voltage soft turning-off and the zero-voltage output diode turning-on.
When the converter operates at CCVM, an additional DC component appears in the input capacitor voltage $v_{CI}$ due to the capacitor current $i_{CI}$. Hence, the average input capacitor voltage $\langle v_C \rangle$ and the average capacitor current $\langle i_{CI} \rangle$ during CCVM is presented as:

$$\langle v_{CI}(t) \rangle = V_{CI} = \frac{V_o}{D} = V_m$$  \hspace{1cm} (3.26)

$$\langle i_{CI}(t) \rangle = I_{CI} = I_1 - DI_2$$  \hspace{1cm} (3.27)

The derivation is shown in Appendix C.3

On the other hand, the input capacitor voltage/current during DCVM can be represented as follows:

$$V_{CI} = \frac{V_o}{D_1} = \frac{V_m}{D + D_1}$$  \hspace{1cm} (3.28)

$$I_{CI} = I_1 (D + D_1) - D_1 I_2$$  \hspace{1cm} (3.29)

The derivation is shown in Appendix C.4

The boundary condition between CCVM and DCVM occurs when the duty cycle $D$ and the normalized discharge time $D_1$ are equal, as per Fig. 3.7. The input capacitor voltage $v_{CI}$ is reflected at the input and the output terminals of the switching network as per eq. (3.28).

An averaged steady-state CCVM and DCVM model is shown in Fig. 3.12. When the converter is working in the DCVM operation, the charging current $\langle i_C(t) \rangle$ through the input capacitor $C_I$ is zero over one switching cycle. Hence, the input capacitor voltage $v_{CI}$ is zero to, the dependent voltage-sources of Fig. 3.12 are deactivated (short circuited). Also, since the charging current of the input capacitor is zero, the upper independent current-sources along with the capacitor are deactivated (open circuited). This is converting the DCVM and CCVM equivalent circuit of Fig. 3.12 to the DCVM equivalent circuit of Fig. 3.11.
3.6 Averaged Input and Output Voltages

The circuit shown in Fig. 3.4 can be represented using an averaged steady-state model (low-frequency model), as shown in Fig. 3.11. The input voltage \( v_1(t) \) and output voltage \( v_2(t) \) have been averaged over one switching cycle \( T_s \).

\[
M = \left( \frac{V_2}{V_1} \right) = \left( \frac{I_2}{I_1} \right) = \frac{D_1}{D'_1 + D_1} \tag{3.21}
\]

\( V_{in} \) equals \( V_c \) over a switching cycle as shown in Fig. 3.8,

\[
V_{in} = V_1 = \frac{1}{2} D_1 V_{CM} + \frac{1}{2} D_3 V_{CM} \tag{3.22}
\]

\[
V_O = V_2 = \frac{1}{2} D_1 V_{CM} \tag{3.23}
\]

\[
\langle v_1(t) \rangle = V_1 = \frac{I_1}{2C_1} T_s \left( D' + D_1 \right) \tag{3.24}
\]

\[
\langle v_2(t) \rangle = V_2 = \frac{I_1}{2C_1} T_s D' D_1 \tag{3.25}
\]

The derivation is shown in Appendix C.2

3.7 Averaged Large-Signal Model for DCVM & CCVM

The steady-state averaged DCVM model, shown in Fig. 3.11, has replaced the switching network of the proposed topology of Fig. 3.4 by two voltage-dependent sources which is valid for DCVM only. Moreover, it is possible also to get a complete model valid for DCVM and continuous capacitor voltage mode (CCVM). [16, 9]

![Fig. 3.11: Large-signal averaged DCVM model (Low-Frequency Model).](image)
When the converter operates at CCVM, an additional DC component appears in the input capacitor voltage $v_{Cl}$ due to the capacitor current $i_{Cl}$. Hence, the average input capacitor voltage $v_C$ and the average capacitor current $i_{Cl}$ during CCVM is presented as:

$$\langle v_{Cl}(t) \rangle = V_{Cl} = \frac{V_o}{D} = V_m$$

$$\langle i_{Cl}(t) \rangle = I_{Cl} = I_1 - DI_2$$

(3.26) (3.27)

The derivation is shown in Appendix C.3

On the other hand, the input capacitor voltage/current during DCVM can be represented as follows:

$$V_{Cl} = \frac{V_o}{D_l} = \frac{V_m}{D^*+D_l}$$

$$I_{Cl} = I \left( D^*+D_l \right) - D_l I_2$$

(3.28) (3.29)

The derivation is shown in Appendix C.4

The boundary condition between CCVM and DCVM occurs when the duty cycle $D$ and the normalized discharge time $D_l$ are equal, as per Fig. 3.7. The input capacitor voltage $v_{Cl}$ is reflected at the input and the output terminals of the switching network as per eq. (3.28).

An averaged steady-state CCVM and DCVM model is shown in Fig. 3.12. When the converter is working in the DCVM operation, the charging current $\langle i_C(t) \rangle$ through the input capacitor $C_l$ is zero over one switching cycle. Hence, the input capacitor voltage $v_{Cl}$ is zero to, the dependent voltage-sources of Fig. 3.12 are deactivated (short circuited). Also, since the charging current of the input capacitor is zero, the upper independent current-sources along with the capacitor are deactivated (open circuited). This is converting the DCVM and CCVM equivalent circuit of Fig. 3.12 to the DCVM equivalent circuit of Fig. 3.11.
3.6 Averaged Input and Output Voltages

The circuit shown in Fig. 3.4 can be represented using an averaged steady-state model (low-frequency model), as shown in Fig. 3.11. The input voltage $v_1(t)$ and output voltage $v_2(t)$ have been averaged over one switching cycle $T_s$.

$$ M = \left( \frac{V_2}{V_1} \right) = \left( \frac{I_1}{I_2} \right) = \frac{D_1}{D'+D_1} \quad (3.21) $$

$V_{in}$ equals $V_c$ over a switching cycle as shown in Fig. 3.8,

$$ V_m = V_1 = \frac{1}{2} D_1 V_{CM} + \frac{1}{2} D_3 V_{CM} \quad (3.22) $$

$$ V_o = V_2 = \frac{1}{2} D_1 V_{CM} \quad (3.23) $$

$$ \langle v_1(t) \rangle = V_1 = \frac{I_1}{2C_1} T_s D'(D'+D_1) \quad (3.24) $$

$$ \langle v_2(t) \rangle = V_2 = \frac{I_1}{2C_1} T_s D D_1 \quad (3.25) $$

The derivation is shown in Appendix C.2

3.7 Averaged Large-Signal Model for DCVM & CCVM

The steady-state averaged DCVM model, shown in Fig. 3.11, has replaced the switching network of the proposed topology of Fig. 3.4 by two voltage-dependent sources which is valid for DCVM only. Moreover, it is possible also to get a complete model valid for DCVM and continuous capacitor voltage mode (CCVM). [16, 9]

![Fig. 3.11: Large-signal averaged DCVM model (Low-Frequency Model).](image)
Taking into account that the input voltage $v_{in}$ is a sinusoidal function. When $V_o << v_{in}$, then the effective input resistance $R_{t-eff}$ will be constant during the line period. Which implies that the proposed converter is suitable for PFC during DCVM.

3.9 Input Current

The rectified input AC voltage is presented as,

$$v_{m}(t) = V_m \sin\left(\frac{2\pi}{T_L} t\right)$$  \hspace{1cm} (3.33)

Where $V_m$ is the peak value of the input voltage, and $f_L$ is the AC line frequency. The time-varying rectified input current $i_l(t)$ is calculated by dividing eq. (3.33) by eq. (3.32),

$$i_l(t) = \frac{2C}{T_L} \frac{V_m}{D^2} \left(\sin\left(\frac{2\pi}{T_L} t\right) - M\right)$$  \hspace{1cm} (3.34)

assuming that the input current $i_l$ is constant over the switching cycle.

Equation (3.34) shows that the input current $i_l(t)$ is purely sinusoidal minus a DC gain equals to $M$. Harmonics appear in the input AC current because of $M$.

3.10 Voltage Conversion “Gain” Ratio

The voltage conversion ratio $M_{dc}$ for a buck converter operating in CCVM is expressed as shown below,

$$M_{dc} = \frac{V_o}{V_m} = D$$  \hspace{1cm} (3.35)

The voltage conversion ratio $M$ in DCVM operation can be found in terms of component parameters by substituting eq. (3.33) and eq. (3.34) in the energy balance over the half line frequency.

Input energy over a half-line cycle is calculated as follows,

$$E_m = \int_{0}^{\tau_L/2} v_{m}(t) i_l(t) dt$$  \hspace{1cm} (3.36)
On the other hand, when the converter is operating in CCVM, the following formulas are applicable from Fig. 3.12:

\[
V_m = \frac{I}{2C_1} T_s D' + V_{C1} \\
V_o = \frac{I}{2C_1} T_s D' D + D V_{C1}
\]  

(3.30)  
(3.31)

The derivation is shown in Appendix C.5

3.8 Effective Input Resistance

The switching network shown in Fig. 3.12 has an effective input resistance that can be obtained from the steady-state averaged DCVM model (low-frequency model) shown in Fig. 3.11 by dividing eq. (3.24) by \(I_{in}\),

\[
R_{r\text{-eff}} = \frac{V_m}{I_m} = \frac{D^2 T_s V_m}{2C_1 \left( \frac{V_m}{V_m - V_o} \right)}
\]  

(3.32)

The derivation is shown in Appendix C.6
3.11 Normalized Discharging Time

The normalized discharging time $D_I$ for the input capacitor $C_i$ is calculated by:

$$D_I = \frac{\eta K}{2D'} \left( 1 + \sqrt{1 + \frac{4D'^2}{\eta K}} \right)$$

(3.43)

The derivation is shown in Appendix C.9.

Since the input voltage is AC, the normalized discharge time $D_I$ becomes a function of time,

$$d_I(t) = D' \left( \frac{M}{\sin(\omega t)} - M \right)$$

(3.44)

The derivation is shown in Appendix C.10.

From eq. 3.44 it can be shown that the normalized discharge time varies over the AC line frequency. The boundary condition between DCVM and CCVM occurs at $d_I(t) = D$ and at $\omega t = \pi/2$, which lead to the same result of eq. (3.35) and eq. (3.40).

---

Fig. 3.13: Conversion ratio ($M$) versus duty cycle ($D$) at 100% Efficiency.

Fig. 3.13 shows the relationship between conversion ratio $M$ and duty cycle $D$ at different values of $K$ at 100% efficiency. DCVM border as dashed lines where $\pi/30 \leq \omega t \leq \pi/2$. The smaller conduction parameter $K$, the wider occurrence range of DCVM.
\[ E_m = \frac{C_1 T_L}{2 T_S D^2} \left( V_m^2 - \frac{4 V_m V_o}{\pi} \right) \]  
(3.37)

The derivation is shown in Appendix C.7

On the other hand, the output energy over a half-line cycle is calculated as follows:

\[ E_o = \int_0^{T_L} V_o i_2(t) \, dt = \frac{V_o^2 T_L}{2 R_L} \]  
(3.38)

The efficiency \( \eta \) is given by,

\[ \eta = \frac{P_o}{P_{in}}. \]

However, the efficiency \( \eta \) can be found from the relationship between the input energy \( E_{in} \) and the output energy \( E_o \) as follows:

\[ \eta = \frac{E_o}{E_{in}} \]  
(3.39)

By substituting eqs. (3.37) and (3.38) in eq. (3.39), the gain \( M \) can be expressed as,

\[ M = \frac{\eta K}{\pi D^2} \left( \sqrt{1 + \frac{\pi^2 D^2}{2 \eta K} - 1} \right) \]  
(3.40)

where \( K \) is a conduction parameter (unit-less) constant,

\[ K = \frac{2 C_1 R_L}{T_S} \]  
(3.41)

The derivation is shown in Appendix C.8

Also, the gain ratio \( M \) can be found using the normalized discharging time \( D_1 \), by substituting eqs. (3.24) and (3.25) as follows:

\[ M = \frac{V_o}{V_m} = \frac{D_1}{D^4 + D_1} \]  
(3.42)

To ensure operation in DCVM mode, \( M \) must be less than \( M_{dc} \).
The input rms current $I_{1\,(\text{rms})}$ can be calculated by,

$$I_{1\,(\text{rms})} = \sqrt{\frac{2}{T_L} \int_0^{T_L} i_1^2(t) \, dt} = \frac{C_1 V_m}{T_S D^2} \left( \sqrt{2 - \frac{16}{\pi} M + 4 M^2} \right)$$  \hspace{1cm} (3.47)

The derivation is shown in Appendix C.12

On the other hand, the average input power over one-half cycle is expressed by,

$$P_{in} = \frac{2}{T_L} E_m = \frac{C_1 V_m^2}{T_S D^2} \left( 1 - \frac{4}{\pi} M \right)$$  \hspace{1cm} (3.48)

The derivation is shown in Appendix C.13

Substituting eqs. (3.47) and (3.48) in eq. (3.46) yields,

$$PF = \frac{1 - \frac{4}{\pi} M}{\sqrt{1 - \frac{8}{\pi} M + 2M^2}}$$  \hspace{1cm} (3.49)

The derivation is shown in Appendix C.14

Note that, as $M$ increases, the power factor is decreased. In other words, as the output voltage $V_o$ decreases, the dead angles (where $V_o$ is bigger than $v_{in}$) of the input AC line current become narrower. This leads to less distorted input AC current, and better power factor.

### 3.14 Components’ Stresses

Voltage stress on the switches is relatively large during DCVM, which is considered as a disadvantage of the DCVM operation. On the hand, operation in DCVM offers relatively low current stresses on the semiconductor components, because the current through the components are clamped to either the input current or the output current. The voltage and current stresses of the converter components are shown in Table 4. The peak voltage stresses are normalized to the output voltage $V_o$, and the rms current stresses are normalized to the load current $I_o$.  

35
over the AC line cycle. In other words, the smaller the value of $K$, the deeper operation in DCVM. However, the disadvantage of operating deeply in DCVM is the high voltage stress at the active switches and the output diode. Hence, $K$ must be selected wisely to insure DCVM operation with acceptable voltage stress values.

### 3.12 Boundary Condition between DCVM & CCVM

The boundary condition between CCVM and DCVM occurs when the duty cycle $D$ and the normalized discharge time $D_1$ are equal, as shown in Fig. 3.14. DCVM will take place once $D_1$ is less than $D$.

![Fig. 3.14: Voltage across the input capacitor $v_{CI}$ in the boundary condition.](image)

Eq. (3.43) is applicable for $D_1 \leq D$. That if $D_1 \geq D$ then the converter enters the CCVM in which $D_1 = D$.

Based on that the boundary condition, $K_{Cre}$ is expressed as,

$$K_{Cre} = \frac{D^2 D'}{\eta}$$

(3.45)

The derivation is shown in Appendix C.11

The conduction parameter $K$ must be less than $K_{Cre}$ to operate in DCVM.

### 3.13 Power Factor Calculations

The power factor can be defined as the ratio of the input power $P_{in}$ to the product of input rms voltage $V_{in (rms)}$ and the input rms current $I_{I (rms)}$. 

Fig. 3.15: First subinterval, \(0 \leq t \leq D_1 T_z\), Switch \(Q_1\) is ON.

\[
v_{L1}(t) = L_1 \frac{d}{dt} i_1(t) = v_i(t) - v_C(t) \tag{3.50}
\]

\[
v_{L0}(t) = L_0 \frac{d}{dt} i_2(t) = v_C(t) - v_0(t) \tag{3.51}
\]

\[
i_{C1}(t) = C_1 \frac{d}{dt} v_C(t) = i_1(t) - i_2(t) \tag{3.52}
\]

\[
i_{C0}(t) = C_0 \frac{d}{dt} v_0(t) = i_2(t) - \frac{v_0(t)}{R_L} \tag{3.53}
\]

Second subinterval, \((D_1 T_z \leq t \leq D T_z)\), switch \(Q_1\) is still turned on, as shown in Fig. 3.16 (DCVM operation).

Fig. 3.16: Second subinterval, \((D_1 T_z \leq t \leq D T_z)\), Switch \(Q_1\) is still ON (DCVM operation).

\[
v_{L1}(t) = L_1 \frac{d}{dt} i_1(t) = v_i(t) \tag{3.54}
\]

\[
v_{L0}(t) = L_0 \frac{d}{dt} i_2(t) = -v_0(t) \tag{3.55}
\]

\[
i_{C1}(t) = C_1 \frac{d}{dt} v_C(t) = i_1(t) - i_2(t) = 0 \tag{3.56}
\]

where \(i_1(t) = i_2(t)\), and

\[
i_{C0}(t) = C_0 \frac{d}{dt} v_0(t) = i_2(t) - \frac{v_0(t)}{R_L} \tag{3.57}
\]
Table 4: Current and voltage stresses.

<table>
<thead>
<tr>
<th></th>
<th>Normalized Peak Voltage ((V_{in}/V_o))</th>
<th>Normalized Effective Current ((I_{rms}/I_o))</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Q_1, Q_2)</td>
<td>(\frac{2}{D'} \left( \frac{1-M}{M} \right))</td>
<td>(\frac{K}{2MD'^2} \sqrt{2-\frac{16}{\pi} M + 4M^2} )</td>
</tr>
<tr>
<td>(D_o)</td>
<td>(\frac{2}{D'} \left( \frac{1-M}{M} \right))</td>
<td>(\frac{K}{MD'^2} \sqrt{\frac{M^2 D'^3}{\pi K} \cdot \frac{2MD'^2}{K} + \frac{M^2D'^3}{K} + \frac{1}{2} \frac{4}{\pi} M + M} )</td>
</tr>
<tr>
<td>(C_1, C_2)</td>
<td>(\frac{2}{D'} \left( \frac{1-M}{M} \right))</td>
<td>(\frac{2K}{MD'} \sqrt{\frac{1}{2} - \frac{4}{\pi} M + M^2} )</td>
</tr>
<tr>
<td>(C_o)</td>
<td>1</td>
<td>---</td>
</tr>
<tr>
<td>(L_1, L_2)</td>
<td>---</td>
<td>(\frac{K}{2MD'^2} \sqrt{2-\frac{16}{\pi} M + 4M^2} )</td>
</tr>
<tr>
<td>(L_o)</td>
<td>---</td>
<td>1</td>
</tr>
</tbody>
</table>

3.15 AC Modeling

In this section, the proposed topology is analyzed to derive a small-signal AC model. The analysis starts by determining the voltage and current waveforms of the inductors and capacitors, and assumes that the output voltage of the converter contains a small switching ripple. In other words, there is low-frequency component (fundamental), and high-frequency component (ripple). Hence, the essential AC waveforms are modeled with the switching ripple ignored [3].

3.15.1 Voltage and Current of the Inductors and Capacitors

To derive a small-signal AC model, the voltage and current waveforms of the inductors and capacitors over one switching cycle are expressed as function of duty cycle \(d(t)\).

- First subinterval \(0 \leq t \leq D_1T_2\), switch \(Q_1\) is turned on, as shown in Fig. 3.15.
\[
\langle i_{Co}(t) \rangle_{T_3} = C_o \frac{d}{dt} \langle \frac{v_o(t)}{T_3} \rangle = \langle i_2(t) \rangle_{T_3} - \langle \frac{v_o(t)}{R_L} \rangle_{T_3} \quad (3.65)
\]

- Second subinterval, \((D_1 T_i \leq t \leq D_i T)\), switch \(Q_i\) is still turned on, as shown in Fig. 3.16 (DCVM operation).

\[
\langle v_{L1}(t) \rangle_{T_3} = L_1 \frac{d}{dt} \langle \frac{i_1(t)}{T_3} \rangle = \langle v_i(t) \rangle_{T_3} \quad (3.66)
\]

\[
\langle v_{Lo}(t) \rangle_{T_3} = L_o \frac{d}{dt} \langle \frac{i_2(t)}{T_3} \rangle = -\langle v_o(t) \rangle_{T_3} \quad (3.67)
\]

\[
\langle i_{C1}(t) \rangle_{T_3} = C_1 \frac{d}{dt} \langle \frac{v_c(t)}{T_3} \rangle = \langle i_1(t) \rangle_{T_3} - \langle i_2(t) \rangle_{T_3} = 0 \quad (3.68)
\]

where, \(\langle i_1(t) \rangle_{T_3} = \langle i_2(t) \rangle_{T_3}\)

\[
\langle i_{Co}(t) \rangle_{T_3} = C_o \frac{d}{dt} \langle \frac{v_o(t)}{T_3} \rangle = \langle i_2(t) \rangle_{T_3} - \langle \frac{v_o(t)}{R_L} \rangle_{T_3} \quad (3.69)
\]

- Third subinterval, \((D_3 T_i \leq t \leq T_3)\), switch \(Q_i\) is turned off, as shown in Fig. 3.17.

\[
\langle v_{L1}(t) \rangle_{T_3} = L_1 \frac{d}{dt} \langle \frac{i_1(t)}{T_3} \rangle = \langle v_i(t) \rangle_{T_3} - \langle v_c(t) \rangle_{T_3} \quad (3.70)
\]

\[
\langle v_{Lo}(t) \rangle_{T_3} = L_o \frac{d}{dt} \langle \frac{i_2(t)}{T_3} \rangle = -\langle v_o(t) \rangle_{T_3} \quad (3.71)
\]

\[
\langle i_{C1}(t) \rangle_{T_3} = C_1 \frac{d}{dt} \langle \frac{v_c(t)}{T_3} \rangle = \langle i_1(t) \rangle_{T_3} \quad (3.72)
\]

\[
\langle i_{Co}(t) \rangle_{T_3} = C_o \frac{d}{dt} \langle \frac{v_o(t)}{T_3} \rangle = \langle i_2(t) \rangle_{T_3} - \langle \frac{v_o(t)}{R_L} \rangle_{T_3} \quad (3.73)
\]

### 3.15.3 Averaging of Waveforms

The low-frequency average of the inductors' voltages and the capacitors' currents are determined by evaluating equations from (3.62) to (3.73) during the first and second subintervals.
Third subinterval, \((DT_3 \leq t \leq T_3)\), switch \(Q_f\) is turned off, as shown in Fig. 3.17.

Fig. 3.17: Third subinterval, \((DT_3 \leq t \leq T_3)\), Switch \(Q_f\) is OFF.

\[ v_{L1}(t) = L_1 \frac{d}{dt} i(t) = v_1(t) - v_C(t) \]  
(3.58)

\[ v_{Lo}(t) = L_o \frac{d}{dt} i_2(t) = -v_o(t) \]  
(3.59)

\[ i_{C1}(t) = C_1 \frac{d}{dt} v_C(t) = i_1(t) \]  
(3.60)

\[ i_{Co}(t) = C_o \frac{d}{dt} v_O(t) = i_2(t) - \frac{v_O(t)}{R_L} \]  
(3.61)

### 3.15.2 Applying Small-Ripple Approximation

To apply the small-ripple approximation, the quantities \(v_{L1}(t)\), \(v_{Lo}(t)\), \(v_o(t)\), \(v_C(t)\), \(i_1(t)\), \(i_2(t)\), \(i_{Co}(t)\) and \(i_{C1}(t)\) are replaced with their low-frequency averaged values \(\langle v_{L1}(t) \rangle_{T_3}\), \(\langle v_{Lo}(t) \rangle_{T_3}\), \(\langle v_o(t) \rangle_{T_3}\), \(\langle v_C(t) \rangle_{T_3}\), \(\langle i_1(t) \rangle_{T_3}\), \(\langle i_2(t) \rangle_{T_3}\), \(\langle i_{Co}(t) \rangle_{T_3}\) and \(\langle i_{C1}(t) \rangle_{T_3}\). [3]

Hence, equations (3.50) to (3.61) become as follows:

First subinterval, \((0 \leq t \leq DT_3)\), switch \(Q_f\) is turned on, as shown in Fig. 3.15.

\[ \langle v_{L1}(t) \rangle_{T_3} = L_1 \frac{d}{dt} \langle i(t) \rangle_{n} = \langle v_1(t) \rangle_{T_3} - \langle v_C(t) \rangle_{T_3} \]  
(3.62)

\[ \langle v_{Lo}(t) \rangle_{T_3} = L_o \frac{d}{dt} \langle i_2(t) \rangle_{n} = \langle v_o(t) \rangle_{T_3} - \langle v_o(t) \rangle_{T_3} \]  
(3.63)

\[ \langle i_{C1}(t) \rangle_{T_3} = C_1 \frac{d}{dt} \langle v_C(t) \rangle_{n} = \langle i_1(t) \rangle_{T_3} - \langle i_2(t) \rangle_{T_3} \]  
(3.64)
\[ \langle i_{c_0}(t) \rangle_{T_s} = C_o \frac{d \langle v_o(t) \rangle_{T_s}}{dt} = \langle i_2(t) \rangle_{T_s} - \frac{\langle v_o(t) \rangle_{T_s}}{R_L} \] (3.65)

- Second subinterval, \((D_1 T_s \leq t \leq DT),\) switch \(Q_1\) is still turned on, as shown in Fig. 3.16 (DCVM operation).

\[ \langle v_{L_1}(t) \rangle_{T_s} = L_1 \frac{d \langle i_1(t) \rangle_{T_s}}{dt} = \langle v_1(t) \rangle_{T_s} \] (3.66)

\[ \langle v_{L_0}(t) \rangle_{T_s} = L_0 \frac{d \langle i_2(t) \rangle_{T_s}}{dt} = -\langle v_o(t) \rangle_{T_s} \] (3.67)

\[ \langle i_c(t) \rangle_{T_s} = C_1 \frac{d \langle v_c(t) \rangle_{T_s}}{dt} = \langle i_1(t) \rangle_{T_s} - \langle i_2(t) \rangle_{T_s} = 0 \] (3.68)

where, \(\langle i_1(t) \rangle_{T_s} = \langle i_2(t) \rangle_{T_s}\)

\[ \langle i_{c_0}(t) \rangle_{T_s} = C_o \frac{d \langle v_o(t) \rangle_{T_s}}{dt} = \langle i_2(t) \rangle_{T_s} - \frac{\langle v_o(t) \rangle_{T_s}}{R_L} \] (3.69)

- Third subinterval, \((DT_s \leq t \leq T_d),\) switch \(Q_1\) is turned off, as shown in Fig. 3.17.

\[ \langle v_{L_1}(t) \rangle_{T_s} = L_1 \frac{d \langle i_1(t) \rangle_{T_s}}{dt} = \langle v_1(t) \rangle_{T_s} - \langle v_c(t) \rangle_{T_s} \] (3.70)

\[ \langle v_{L_0}(t) \rangle_{T_s} = L_0 \frac{d \langle i_2(t) \rangle_{T_s}}{dt} = -\langle v_o(t) \rangle_{T_s} \] (3.71)

\[ \langle i_c(t) \rangle_{T_s} = C_1 \frac{d \langle v_c(t) \rangle_{T_s}}{dt} = \langle i_1(t) \rangle_{T_s} \] (3.72)

\[ \langle i_{c_0}(t) \rangle_{T_s} = C_o \frac{d \langle v_o(t) \rangle_{T_s}}{dt} = \langle i_2(t) \rangle_{T_s} - \frac{\langle v_o(t) \rangle_{T_s}}{R_L} \] (3.73)

**3.15.3 Averaging of Waveforms**

The low-frequency average of the inductors' voltages and the capacitors' currents are determined by evaluating equations from (3.62) to (3.73) during the first and second subintervals.
Third subinterval, \( DT_s \leq t \leq T_3 \), switch \( Q_I \) is turned off, as shown in Fig. 3.17.

\[
\begin{align*}
  v_{L1}(t) &= L_1 \frac{d}{dt} i_{L1}(t) = v_1(t) - v_c(t) \\
v_{L0}(t) &= L_o \frac{d}{dt} i_{L0}(t) = -v_o(t) \\
i_{c1}(t) &= C_1 \frac{d}{dt} v_c(t) = i_1(t) \\
i_{co}(t) &= C_o \frac{d}{dt} v_o(t) = i_2(t) - \frac{v_o(t)}{R_L}
\end{align*}
\]

**3.15.2 Applying Small-Ripple Approximation**

To apply the small-ripple approximation, the quantities \( v_{L1}(t), v_{L0}(t), v_o(t), v_c(t), v_f(t), i_1(t), i_2(t), i_{co}(t) \) and \( i_{c1}(t) \) are replaced with their low-frequency averaged values \( \langle v_{L1}(t) \rangle_{T_s}, \langle v_{L0}(t) \rangle_{T_s}, \langle v_o(t) \rangle_{T_s}, \langle v_c(t) \rangle_{T_s}, \langle v_f(t) \rangle_{T_s}, \langle i_1(t) \rangle_{T_s}, \langle i_2(t) \rangle_{T_s}, \langle i_{co}(t) \rangle_{T_s} \) and \( \langle i_{c1}(t) \rangle_{T_s} \). \[3\]

Hence, equations (3.50) to (3.61) become as follows:

First subinterval, \( 0 \leq t \leq D_f T_2 \), switch \( Q_I \) is turned on, as shown in Fig. 3.15.

\[
\begin{align*}
  \langle v_{L1}(t) \rangle_{T_s} &= L_1 \frac{d}{dt} \langle i_{L1}(t) \rangle_{T_s} = \langle v_1(t) \rangle_{T_s} - \langle v_c(t) \rangle_{T_s} \\
  \langle v_{L0}(t) \rangle_{T_s} &= L_o \frac{d}{dt} \langle i_{L0}(t) \rangle_{T_s} = \langle v_o(t) \rangle_{T_s} - \langle v_o(t) \rangle_{T_s} \\
  \langle i_{c1}(t) \rangle_{T_s} &= C_1 \frac{d}{dt} \langle v_c(t) \rangle_{T_s} = \langle i_1(t) \rangle_{T_s} - \langle i_2(t) \rangle_{T_s}
\end{align*}
\]
Linearization of the Input Inductor

a) The resulting DC terms are,

\[ V_1 - (1 - D + D_1) V_c = 0 \]  \hspace{1cm} (3.79)

b) The linearized 1st order AC terms are,

\[ L \frac{d\hat{i}_1(t)}{dt} = \hat{v}_1(t) - (1 - D + D_1) \hat{v}_c(t) + \left[ \tilde{d}(t) - \hat{d}_1(t) \right] V_c \]  \hspace{1cm} (3.80)

The derivation is shown in Appendix C.19

Linearization of the Output Inductor

a) The resulting DC terms are,

\[ D_1 V_c - V_o = 0 \]  \hspace{1cm} (3.81)

b) The linearized 1st order AC terms are,

\[ L_o \frac{d\hat{i}_2(t)}{dt} = D_1 \hat{v}_c(t) + \hat{d}_1(t) V_c - \hat{v}_o(t) \]  \hspace{1cm} (3.82)

The derivation is shown in Appendix C.20

Linearization of the Input Capacitor

a) The resulting DC terms are,

\[ I_1 (1 - D + D_1) - D_1 I_2 = 0 \]  \hspace{1cm} (3.83)

b) The linearized 1st order AC terms are,

\[ C \frac{d\hat{v}_c(t)}{dt} = -\hat{d}(t)(I_1 + \hat{d}_1(t)(I_1 - I_2) + (1 - D + D_1)\hat{v}_i(t) - D_1 \hat{i}_2(t) \]  \hspace{1cm} (3.84)

The derivation is shown in Appendix C.21

Linearization of the Output Capacitor

a) The resulting DC terms are,

\[ I_2 \frac{V_o}{R_L} = 0 \]  \hspace{1cm} (3.85)

b) The linearized 1st order AC terms are,
Averaging Input Inductor

\[
\langle v_{Li}(t) \rangle_T = L_I \frac{d\langle i_{Li}(t) \rangle_T}{dt} = \langle v_i(t) \rangle_T - \langle v_c(t) \rangle_T \left[ 1 - d(t) + d_1(t) \right]
\]

The derivation is shown in Appendix C.15

Averaging Output Inductor

\[
\langle v_{Lo}(t) \rangle_T = d_i(t) \langle v_c(t) \rangle_T - \langle v_o(t) \rangle_T
\]

The derivation is shown in Appendix C.16

Averaging Input Capacitor

\[
\langle i_{Cl}(t) \rangle_T = C_I \frac{d\langle v_c(t) \rangle_T}{dt} = \langle i_i(t) \rangle_T \left[ 1 - d(t) + d_1(t) \right] - \langle i_2(t) \rangle_T d_1(t)
\]

The derivation is shown in Appendix C.17

Averaging Output Capacitor

\[
\langle i_{Co}(t) \rangle_T = C_o \frac{d\langle v_o(t) \rangle_T}{dt} = \langle i_i(t) \rangle_T - \frac{\langle v_o(t) \rangle_T}{R_L}
\]

The derivation is shown in Appendix C.18

3.15.4 Perturbation and Linearization

Equations (3.74), (3.75), (3.76) and (3.77) are non-linear equations. Multiplication of the time-varying signals generate high order AC terms. By neglecting the high order AC terms, the desired equations can be expressed as follows:

\[
\begin{align*}
\langle v_i(t) \rangle_T &= V_i + \hat{v}_i(t), \\
\langle v_{Li}(t) \rangle_T &= V_{Li} + \hat{v}_{Li}(t), \\
\langle v_c(t) \rangle_T &= V_c + \hat{v}_c(t), \\
\langle v_{Lo}(t) \rangle_T &= V_{Lo} + \hat{v}_{Lo}(t), \\
\langle v_c(t) \rangle_T &= V_{Co} + \hat{v}_{Co}(t), \\
\langle v_o(t) \rangle_T &= V_o + \hat{v}_o(t), \\
\langle i_i(t) \rangle_T &= I_i + \hat{i}_i(t), \\
\langle i_{Cl}(t) \rangle_T &= I_{Cl} + \hat{i}_{Cl}(t), \\
\langle i_o(t) \rangle_T &= I_o + \hat{i}_o(t), \\
\langle d(t) \rangle_T &= D + \hat{d}(t),
\end{align*}
\]

The variations are assumed much smaller in magnitude than those of the DC quiescent values such that $|\hat{v}_i(t)| << |V_i|$. By substituting the eqs. (3.78) into the nonlinear equations (3.74), (3.75), (3.76) and (3.77), the nonlinear equations become linearized as will be shown in the next section.
The circuits of Figs. 3.18, 3.19, 3.20 and 3.21 are combined in Fig. 3.22. The dependent sources are replaced by ideal transformers, leading to the desired equivalent circuit of Fig. 3.23 that models the low-frequency small-signal variations in the converter waveforms.

\[ \frac{d^2}{dt^2} \dot{v}_t(t) = C_d \dot{v}_t(t) + L_i \frac{d}{dt} \dot{v}_t(t) + \frac{1}{R_i} \dot{v}_o(t) \]

**Fig. 3.22: Equivalent circuits of Figs. 3.18 to 3.21, collected together.**

\[ \frac{d^2}{dt^2} \dot{v}_t(t) = C_d \dot{v}_t(t) + L_i \frac{d}{dt} \dot{v}_t(t) + \frac{1}{R_i} \dot{v}_o(t) \]

**Fig. 3.23: Small-signal AC equivalent circuit model of the proposed topology.**

### 3.15.6 Analysis of Converter Transfer Functions

The AC output voltage variations \( \dot{v}_o(s) \) can be expressed as the superposition of the two sources. This allows us to derive the analytical expressions and to draw bode plots for the control-to-output \( G_{vd}(s) \) and for the line-to-output \( G_{vg}(s) \) transfer functions for the circuit. Since the converter contains more than one AC source, namely, the line input \( \dot{v}_l(s) \) and the control input \( \dot{d}(s) \), then:

\[
\dot{v}_o(s) = G_{vg}(s) \dot{v}_l(s) + G_{vd}(s) \dot{d}(s)
\]  

(3.87)

where the transfer functions \( G_{vg}(s) \) and \( G_{vd}(s) \) can be defined as,
The derivation is shown in Appendix C.22

### 3.15.5 Construction of the Small-Signal model and Equivalent Circuit

Eqs. (3.80), (3.84), (3.82) and (3.86), respectively, are used to build an averaged small-signal AC model of the proposed topology as demonstrated in Figs. 3.18 to 3.21.
Fig. 3.25: Pushing input voltage and input components towards the output voltage.

Fig. 3.26 shows the simplified equivalent circuit of Fig. 3.25 (c), where

\[
Z_{eq} = \left(sL_o + \left( R_L \parallel \frac{1}{sC_o} \right) \parallel \frac{D_1^2}{sC_1} \right)
\]

Further derivations using eqs. (3.88) and (3.89) yield the line-to-output \( G_{ge}(s) \) transfer function,

\[
G_{ge}(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_i(s)} \bigg|_{\tilde{d}(s) \to 0}
\]

\[
= \frac{\frac{D_1}{1-D+D_1}}{s^4 \frac{L_i L_o C_i C_o}{(1-D+D_1)^2} + s^3 \frac{L_i L_o C_1}{R_L (1-D+D_1)^2} + s^2 \frac{D_1^2 L_i C_o + L_i C_1 + L_o C_o}{(1-D+D_1)^2} + s \frac{D_1^2 L_i}{R_L (1-D+D_1)^2} + \frac{L_o}{R_L} + 1}
\]

The derivation is shown in Appendix C.23
\[ G_{rg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_i(s)} \]
\[ G_{rd}(s) = \frac{\hat{v}_i(s)}{d(s)} \frac{\hat{v}_y(s) = 0}{\hat{v}_r(s) = 0} \]

3.15.6.1 Line-to-Output Transfer Function

In order to find the line-to-output \( G_{rg}(s) \) transfer function, we deactivate the \( \hat{d}(s) \) sources in Fig. 3.23 to become as shown in Fig. 3.24,

Fig. 3.24: Deactivating \( \hat{d}(t) \) sources.

The input voltage source and the input components are then pushed towards the output voltage \( \hat{v}_o(s) \) as shown in Figs. 3.25 (a-c).

(a) \[
\frac{1}{(1-D+D_i)^2} \hat{v}_i(s)
\]

(b) \[
\frac{D_i}{(1-D+D_i)} \hat{v}_i(s)
\]
Fig. 3.28: Pushing $d^2$-dependent voltage source, $d^2$-dependent current source and input components towards the output voltage.

Next, we apply the superposition technique to the circuit in Fig. 3.28(c). First, the $d$ - dependent current source is deactivated as shown in Fig. 3.29.

Fig. 3.29: Equivalent circuit with the $d^2$-dependent current source deactivated.

Fig. 3.30 shows the simplified equivalent circuit of Fig. 3.29 where

$$Z_{eq} = \left( sL + \left( R_L \parallel \frac{1}{sC} \right) \right) \parallel \frac{D_l^2}{sC}$$

(3.91)

Fig. 3.30: A simplified equivalent circuit showing $Z_{eq}$. 

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3.15.6.2 Control-to-Output Transfer Function

The control-to-output $G_{vd}(s)$ transfer function is found by deactivating all the $\hat{v}_i(s)$ sources in Fig. 3.23, as shown in Fig. 3.27.

Then $\hat{d}$-dependent voltage source, $\hat{d}$-dependent current source and input components are pushed towards the output voltage $\hat{v}_o(s)$ as shown in Fig. 3.28 (a-c).
Further derivations using eqs. (3.88) and (3.93) yield the line-to-output $G_{vd}(s)$ transfer function (with the $\hat{d}$-dependent voltage source deactivated),

$$G_{vd}(s) = \frac{\hat{v}_c(s)}{\hat{d}(s)}_{v_{i(b)}=0} = \frac{\left(\frac{D_1}{(1-D+D_1)^2}\right)I_i}{s^4 L_1 L_o C_o C_a + s^3 \frac{L_1 L_o C_a}{(1-D+D_1)^2} + s^2 \left(\frac{D_1^2 L_o C_a + L_1 C_a}{(1-D+D_1)^2} + L_o C_a\right) + s \left(\frac{D_1^2 L_o}{R_L (1-D+D_1)^2} + \frac{L_o}{R_L}\right) + 1}$$

The derivation is shown in Appendix C.25. The control-to-output $G_{vd}(s)$ transfer function is the summation of eqs. (3.92) and (3.94),

$$G_{vd}(s) = \frac{\hat{v}_c(s)}{\hat{d}(s)}_{v_{i(b)}=0} = \frac{\left(\frac{D_1}{(1-D+D_1)^2}\right)I_i + \left(\frac{D_1}{1-D+D_1}\right)I_v}{s^4 L_1 L_o C_o C_a + s^3 \frac{L_1 L_o C_a}{(1-D+D_1)^2} + s^2 \left(\frac{D_1^2 L_o C_a + L_1 C_a}{(1-D+D_1)^2} + L_o C_a\right) + s \left(\frac{D_1^2 L_o}{R_L (1-D+D_1)^2} + \frac{L_o}{R_L}\right) + 1}$$

### 3.15.7 Bode Plot of the Line-to-Output Transfer Function

The bode plot of the line-to-output transfer function, shown in Fig. 3.34, was drawn by entering eq. (3.90) to a MATLAB code shown in Appendix B.1. Considering $D = 0.483$, $L_1 = L_2 = 2.2$ mH, $L_o = 180$ μH, $C_1 = C_2 = 47$ nF, $C_o = 3000$ μF, $R_L = 23$ Ω, $T_s = 20$ μSec, $D_f$ is calculated from eq. (3.43), and $K$ is calculated from eq. (3.41).
Further derivations using eqs. (3.88) and (3.91) yield the line-to-output \( G_{vd}(s) \) transfer function (with the \( d \) - dependent current source deactivated).

\[
G_{vd}(s) = \frac{v_{d}(s)}{d(s)} = \frac{\left( \frac{D_{1}}{1-D+D_{1}} \right) v_{e}}{s^{4} \frac{L_{L}L_{C}C_{o}}{(1-D+D_{1})^{2}} + s^{3} \frac{L_{L}L_{C}}{R_{L}(1-D+D_{1})} + s^{2} \left( \frac{D_{1}^{2}L_{L}C_{o}}{(1-D+D_{1})^{2}} + L_{o}C_{o} \right) + s \left( \frac{D_{1}^{2}L_{L}}{R_{L}(1-D+D_{1})} + \frac{L_{o}}{R_{L}} \right) + 1}
\]

(3.92)

The derivation is shown in Appendix C.24

Now, we deactivate the \( d \) - dependent voltage source in Fig. 3.28(c) as shown in Fig. 3.31.

![Fig. 3.31: Equivalent circuit with the \( d \)-dependent voltage source deactivated.](image)

The equivalent circuit in Fig. 3.31 is simplified using the source transformation technique [43]. The resulting circuit is shown in Fig. 3.32.

![Fig. 3.32: Equivalent circuit after deactivating \( d \)-dependent voltage source.](image)

The simplified equivalent circuit of Fig. 3.32 is shown below in Fig. 3.33.
Chapter 4

Design Procedure and Verification

In this chapter, a step-by-step design procedure of the proposed topology is presented.

4.1 Converter Design

The bridgeless buck converter is designed with the following characteristics:

Table 5: Specifications of the simulated topology.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power $P_o$</td>
<td>100W</td>
</tr>
<tr>
<td>Output voltage $V_o$</td>
<td>48V</td>
</tr>
<tr>
<td>Input voltage $V_{in}$</td>
<td>$141.42 \sin (2\pi 50 t) \ V$</td>
</tr>
<tr>
<td>Switching frequency $f_s$</td>
<td>50kHz</td>
</tr>
<tr>
<td>Efficiency $\eta$</td>
<td>95.64%</td>
</tr>
<tr>
<td>Input Current ripple $\Delta I_{in}$</td>
<td>$10 % I_{in}$</td>
</tr>
<tr>
<td>Output voltage ripple $\Delta V_o$</td>
<td>$0.6 % V_o$</td>
</tr>
</tbody>
</table>

a) Voltage conversion ratio $M_{dc}$ at CCVM is calculated using eq. (3.35),

b) $K_{Cr_c}$ provides the boundary condition limit between DCVM & CCVM and is evaluated from eq. (3.45).

c) For operation in DCVM, $K < K_{Cr_c}$ as mentioned in section 3.11, so let $K = 0.9 K_{Cr_c}$.

d) For a given voltage conversion ratio $M$, the duty cycle $D$ is calculated from eq. (3.40),

$$ D' = \frac{1}{M} \sqrt{\frac{2\eta K}{\pi} \left( \frac{\pi}{4} - M \right)} = 0.516 $$  \hspace{1cm} (4.1)

4.2 Input Capacitors Design

$C_1$ and $C_2$ can be calculated as shown in eq. (4.2),
This transfer function describes the variation of the input voltage $v_{in}(t)$ to the output voltage $v_o(t)$.

### 3.15.8 Bode Plot of the Control-to-Output Transfer Function

The bode plot of the control-to-output transfer function, shown in Fig. 3.35, was drawn by entering eq. (3.95) to a MATLAB code shown in Appendix B.2. $D_I$ is calculated from eq. (3.43), and $K$ is calculated from eq. (3.41). In addition, $v_{Cl}$, $V_o$, and $I_I$ are calculated from eqs. (3.28), (3.26) and (3.21), respectively.

### 3.16 Summary of Key Points

In this chapter, a detailed analysis, based on assumptions of the bridgeless topology, was presented. The closed form equations required for the converter design and component selection have been formulated. Large and small signal models have been developed.
The selection of the output inductor $L_o$ depends on the behavior of the circuit during the switch-on time. To maintain a constant output current during one switching cycle, the resonant frequency of the input capacitor $C_i$ and the equivalent inductors $L_e$ ($L_i // L_o$) must be much smaller than the switching time.

$$L_e >> \frac{1}{C_i} \left( \frac{DT_{\pi}}{2\pi} \right)^2 = 50 \mu H$$ (4.6)

The derivation is shown in Appendix C.28.

Now, assume that $L_e = 165 \mu H$ where

$$L_e = L_i // L_o = \frac{L_i \cdot L_o}{L_i + L_o}$$ (4.7)

Therefore, the output inductor $L_o$ is calculated to be $180 \mu H$.

### 4.5 Output Capacitor Design

The output capacitor $C_o$ is assumed to be large enough such that the output voltage $V_o$ is considered to be constant over one half cycle of the line frequency. $C_o$ value is required to maintain a peak-peak output voltage ripple of 0.6% of $V_o$, and can be evaluated as,

$$C_o = \frac{1}{\Delta V_o} \int_{T_{\pi}/2}^{3T_{\pi}/8} (i_{L_o}(t) - I_o) \, dt$$ (4.8)

where $I_o$ is the load current and $i_{L_o}(t)$ is the output inductor current (Appendix C.29),

$$i_{L_o}(t) = \frac{\eta \cdot V_o}{R_{i_eff} \cdot M^2} \sin^2(\omega t)$$ (4.9)

With reference to Fig (3.4),

$$i_{C_o}(t) = i_{L_o}(t) - I_o$$ (4.10)

Substituting the values of $I_o$ and $i_{L_o}(t)$ and solving the integration yields to,

$$C_o = \frac{T_L \cdot V_o}{4 \Delta V_o} \left[ \frac{\eta}{R_{i_eff} \cdot M^2} \left( \frac{1}{\pi} + \frac{1}{2} \right) - \frac{1}{R_L} \right]$$ (4.11)

The derivation is shown in Appendix C.30. From eq. (4.9) we obtain $C_o \approx 3000 \mu F$.  

53
\[ C_1 = C_2 = \frac{K T_S}{2 R_L} \approx 47 \, nF \]  \hspace{1cm} (4.2)

4.3 Input Current Ripple

The rms input current is calculated using eq. (3.47),

\[ I_{\text{rms}} = \frac{C_1 V_{\text{peak}}}{T_S D^2} \left( \sqrt{2 - \frac{16}{\pi} M + 4 M^2} \right) = 1.065 \, A \]  \hspace{1cm} (4.3)

The input current ripple \( \Delta I_{in} \) as given in the specifications shown in Table 4.1 is

\[ \Delta I_{in} = 10\% I_{\text{rms}} = 0.1065 \, A \]

4.4 Inductors Design

The selection of input inductors \( L_1 \) and \( L_2 \) is based on the desired ripple value of the input current. Therefore, \( L_1 \) and \( L_2 \) can be obtained considering the maximum current ripple.

- \( L_1 \) & \( L_2 \) are calculated as follows:
  a. Lower limit: The inductance of \( L_1 \) & \( L_2 \) must be large enough to maintain continuous input current and, on the other hand, to avoid resonance with the input capacitors \( C_1 \) & \( C_2 \) during switch-off time.

\[ L_1 = L_2 \gg \frac{1}{C_1 \left( \frac{D T_S}{2 \pi} \right)^2} = 57.5 \, \mu H \]  \hspace{1cm} (4.4)

The derivation is shown in Appendix C.26

b. Upper limit: The inductance of \( L_1 \) & \( L_2 \) must not be very large to minimize the phase shift between the input voltage and the input current. Therefore, the reactance of \( L_1 \) must be less than the converter effective input resistance \( R_{\text{eff}} \).

\[ L_1 = L_2 \ll \frac{R_{\text{eff}}}{\omega_L} \geq \frac{D^2 T_S}{4 \pi C_1 f_L} = 185 \, mH \]  \hspace{1cm} (4.5)

The derivation is shown in Appendix C.27

A value of 2.2 \( mH \) is chosen for \( L_1 \) and \( L_2 \).
Chapter 5

Simulation and Experimental Results

This chapter presents the simulation and experimental results for the proposed topology.

5.1 Simulation Results

Real component models are used in the simulation for the diodes and switches. An ultrafast, high voltage diode (STTH5L06) is used for the output diode $D_o$, with a forward voltage drop of 0.85V and 600V/5A ratings. Schottkey diodes (STPS30120CT) for the return diodes $D_p$ and $D_n$ are used. MOSFET (STY60NM60) are used to model the converter active switches. The simulation parameters are: $V_{in} = 100$ V$_{rms}$, $C_1 = C_2 = 47$ nf, $L_1 = L_2 = 2.2$ mH, $L_o = 180$ µH, $C_o = 3000$ µf, $R_L = 23$ Ω, $P_{out} = 100$ W, $f_L = 50$ Hz and $f_s = 50$ kHz. The calculated duty cycle is found to be 48.3%. The proposed topology, shown in Fig. 3.1, is simulated using PSpice 16.3-p008 from Cadence Design Systems Inc. The code is shown in Appendix-A.

5.1.1 Input Voltage and Input Current

The topology is simulated at different loads of 100W, 200W and 300W. The input current $i_m$, input voltage $v_{in}$ and corresponding output voltage $V_o$ waveforms are shown in Fig. 5.1 (a-c) respectively.
4.6 Proposed Converter Components

The discrete components (inductors and capacitors) used in the simulation are ideal, however, the switches and diodes are real models, as shown in Table 6.

Table 6: List of components used in the proposed topology.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value/Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$</td>
<td>2.2 mH</td>
</tr>
<tr>
<td>$L_2$</td>
<td>2.2 mH</td>
</tr>
<tr>
<td>$L_o$</td>
<td>180 $\mu$F</td>
</tr>
<tr>
<td>$C_1$</td>
<td>47 nF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>47 nF</td>
</tr>
<tr>
<td>$C_o$</td>
<td>3000 $\mu$F</td>
</tr>
<tr>
<td>$Q_1, Q_2$</td>
<td>STY60NM60</td>
</tr>
<tr>
<td>$D_m, D_n$</td>
<td>STPS30120CT</td>
</tr>
<tr>
<td>$D_o$</td>
<td>STTH5L06</td>
</tr>
</tbody>
</table>

4.7 Summary of Key Points

Component selection of the converter for a 100W load has been presented.
It can be observed from Fig. 5.1 that the input line current $i_{in}$ is in phase with the input voltage $v_{in}$.

The topology was also simulated at load power value of 100W and different input voltage levels. The waveforms of the input current $i_{in}$, the input voltage $v_{in}$ at 100 $V_{rms}$, 120 $V_{rms}$, and 220 $V_{rms}$ at 48 $V_{dc}$ output voltage $V_o$ are shown in Figs. 5.2 (a-c).
Fig. 5.1: Simulated input current, 100\text{V}_{\text{rms}} input voltage and output voltage for (a) 100W, (b) 200W and (c) 300W loads.
Table 8: Input current harmonics of the proposed DCVM topology.

<table>
<thead>
<tr>
<th>Harmonic Order</th>
<th>Frequency (Hz)</th>
<th>Fourier Component (A)</th>
<th>Normalized Comp. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>50</td>
<td>1.356</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>150</td>
<td>0.1706</td>
<td>0.1258</td>
</tr>
<tr>
<td>5</td>
<td>250</td>
<td>0.06531</td>
<td>0.0481</td>
</tr>
<tr>
<td>7</td>
<td>350</td>
<td>0.06786</td>
<td>0.0500</td>
</tr>
<tr>
<td>9</td>
<td>450</td>
<td>0.05903</td>
<td>0.0435</td>
</tr>
<tr>
<td>11</td>
<td>550</td>
<td>0.02308</td>
<td>0.0170</td>
</tr>
</tbody>
</table>

**Fig. 5.3:** Comparison between input current harmonics of the proposed bridgeless DCVM topology and IEC 61000-3-2 limits for Class D.

**5.1.3 Simulated Curves**

The waveforms of the capacitor voltage and the gating voltage over the switching cycle are shown in Fig. 5.4. It can be observed that they are similar to the theoretical waveforms shown in Fig. 3.10.
5.1.2 Input Line Current Harmonics

To compare the input line current harmonics with IEC 61000-3-2 limits for class D, the input current waveform was analyzed by Fourier using PSpice software. The line current harmonics of the IEC 61000-3-2 limits for Class D are shown in Table 7 below, [1,2]. The line current harmonics of the proposed DCVM topology have been tabulated using PSpice software as shown in Table 8 and Fig. 5.3.

Table 7: Input current harmonics limits of IEC 61000-3-2 (Class D).

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>Maximum permissible harmonic current per Watt mA/W</th>
<th>Maximum permissible harmonic current A</th>
<th>Normalized Comp. (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>3.69</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>3.4</td>
<td>2.3</td>
<td>0.62</td>
</tr>
<tr>
<td>5</td>
<td>1.9</td>
<td>1.14</td>
<td>0.31</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>0.77</td>
<td>0.21</td>
</tr>
<tr>
<td>9</td>
<td>0.5</td>
<td>0.4</td>
<td>0.11</td>
</tr>
<tr>
<td>11</td>
<td>0.35</td>
<td>0.33</td>
<td>0.09</td>
</tr>
<tr>
<td>$13 \leq n \leq 39$ (Odd harmonics only)</td>
<td>3.85/n</td>
<td>0.23 * (8/n)</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 5.2: Simulated waveforms at 100W output power, and input voltages for (a) 100Vrms, (b) 120Vrms and (c) 220Vrms.
The output diode current waveform shown in Fig. 5.7 is similar to the theoretical waveform shown in Fig. 3.10.

The input capacitor current has been simulated and shown in Fig. 5.8.
The waveforms of both of the input capacitors' voltages over the line cycle are shown in Fig. 5.5. It can be observed that they are 180 degrees shifted.

The simulated waveform of the switch current is shown in Fig. 5.6. It can be seen that it is similar to the theoretical waveform shown in Fig. 3.10. However, there is some noise at \( D_I T_s \) and \( D T_s \) which reflects the behavior of the switches' models in the simulation.
Fig. 5.10: Voltage stress across the output diode $D_o$ and control voltage.

Fig. 5.11 shows simulation results of gating voltage, switch current $i_Q$, output diode current $i_{D_o}$, input capacitor current $i_{C_I}$, input capacitor voltage $v_{C_I}$, output diode voltage $v_{D_o}$ and switch voltage $v_Q$. 
Fig. 5.8: Input capacitor current $i_{CI}$ and gating voltage.

Fig. 5.9: Voltage stress across the switch $Q_I$ and control voltage.

The voltage stress across the output diode is shown in Fig. 5.10. It can be observed that it is similar to the theoretical waveform shown in Fig. 3.10. It shows that voltage stress is equal to the input capacitor peak voltage $V_{CM}$. 
Table 9: Parameters of the prototype components.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$ and $L_2$</td>
<td>2.2 mH</td>
<td>Toroidal Inductors (Wilco)</td>
</tr>
<tr>
<td>$L_0$</td>
<td>180 $\mu$H</td>
<td>Toroidal Inductors (Wilco)</td>
</tr>
<tr>
<td>$C_1$ and $C_2$</td>
<td>47 nF, 1000 Vdc</td>
<td>Polypropylene Capacitors. (Low ESR)</td>
</tr>
<tr>
<td>$C_o$</td>
<td>3000 $\mu$F, 250 V</td>
<td>Aluminum Electrolytic Capacitor</td>
</tr>
<tr>
<td>$D_o$</td>
<td>300 V, 10 A, $V_f=0.64$ V</td>
<td>SBR 10U300CT Diode</td>
</tr>
<tr>
<td>$D_p$ and $D_n$</td>
<td>600V, 5A, $V_f=1.05V$</td>
<td>STPS30120CT Schottky diodes</td>
</tr>
<tr>
<td>$Q_1$ and $Q_2$</td>
<td>650V, 60 A, 45 m$\Omega$.</td>
<td>IPW60R045CP MOSFETs</td>
</tr>
</tbody>
</table>

The toroidal configuration provides a closed magnetic field resulting in low EMI [44]. The following sections present the experimental results compared to the same parameters simulated circuit along with the discussion.

5.2.1 Input Voltage and Input Current

The experimental waveforms of the input voltage, input current and output voltage are shown in Fig. 5.12. These results can be compared to the simulated waveforms in Fig 5.1 (a). The experimental waveforms verified the PSpice simulated topology.

![Experimental waveforms](image)

Fig. 5.12: Experimental results for the input current, input voltage and output voltage for a 100W load.
5.2 Experimental Results

The circuit shown in Fig. 3.1 has been built in the lab using the components in Table 9 at an operating point of input voltage \( V_{\text{rms}} = 100 \) V, \( P_{\text{out}} = 100 \) W, \( f_I = 50 \) Hz, \( f_s = 50 \) kHz and duty cycle of 51.5%. 
5.3 Efficiency

The efficiency calculated out of the measured values in the laboratory is 95%, while the efficiency out of the simulation is 95.64% using real components with internal resistances, as shown in Fig. 5.15. The PSpice simulation code is presented in Appendix A.2.

The efficiency, power factor and THD of the proposed topology are compared with a full bridge buck PFC converter’s operating in DCVM [15], shown in Fig. 5.16, at
5.2.2 Input Capacitor Voltage

The waveforms of the input capacitors' voltages over the line cycle are shown in Fig. 5.13. It can be observed that they are shifted by 180 degrees, and \( C_1 \) is operating in the positive half cycle, while \( C_2 \) is operating in the negative half cycle. The capacitor peak voltage is measured to be 385V which is similar to the simulation results of Fig. 5.5.

![Fig. 5.13: Experimental results for input capacitors' voltage over line cycle.](image)

5.2.3 Capacitor Voltage and Current and the Switch Voltage

The waveforms of the voltage across the active switch, and the input capacitor voltage and current over switching cycle are shown in Fig. 5.14.
Table 11 presents a comparison between the efficiency, THD, and power factor of the simulated proposed topology and the simulated conventional full bridge DCVM buck PFC converter at different load values.

5.4 Input Line Current Harmonics

The input current harmonics of the proposed DCVM topology and of the conventional full bridge DCVM buck PFC are compared with the IEC 61000-3-2 limits for Class D as shown in Fig. 5.17 below.

![Input line current harmonics comparison](image)

Fig. 5.17: Input line current harmonics of the proposed topology and conventional full bridge PFC compared to IEC 61000-3-2 standard.

Fig. 5.17 shows that the proposed bridgeless topology yields lower THD and input line current harmonics and better power factor than the conventional full bridge DCVM buck PFC.

5.5 Output Voltage Control

Fig. 5.18 shows the output voltage when duty cycle $D$ is suddenly increased to 0.633.
different universal AC line voltages and different power ratings, as shown in Tables 10 and 11, respectively.

![Diagram of Full bridge buck PFC converter](image)

**Fig. 5.16: Full bridge buck PFC converter operating in DCVM [15].**

**Table 10: Efficiency, PF and THD of the proposed topology.**

<table>
<thead>
<tr>
<th>V&lt;sub&gt;in&lt;/sub&gt; [rms]</th>
<th>P&lt;sub&gt;n&lt;/sub&gt; [W]</th>
<th>Efficiency %</th>
<th>THD %</th>
<th>PF</th>
<th>P&lt;sub&gt;m&lt;/sub&gt; [W]</th>
<th>D</th>
<th>K</th>
<th>K&lt;sub&gt;Cur&lt;/sub&gt;</th>
<th>F&lt;sub&gt;S&lt;/sub&gt; [Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal</td>
<td>Simulated</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90 V</td>
<td>100</td>
<td>93.5</td>
<td>95</td>
<td>20.64</td>
<td>0.979</td>
<td>98.43</td>
<td>0.59</td>
<td>0.092</td>
<td>0.133</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>185</td>
<td>94.5</td>
<td>23.35</td>
<td>0.974</td>
<td>195.7</td>
<td>0.71</td>
<td>0.046</td>
<td>0.133</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>273</td>
<td>92.8</td>
<td>24.09</td>
<td>0.972</td>
<td>294.1</td>
<td>0.763</td>
<td>0.031</td>
<td>0.133</td>
</tr>
<tr>
<td>100V</td>
<td>100</td>
<td>91.66</td>
<td>95.64</td>
<td>15.13</td>
<td>0.989</td>
<td>95.84</td>
<td>0.483</td>
<td>0.092</td>
<td>0.120</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>180</td>
<td>94.5</td>
<td>18.68</td>
<td>0.983</td>
<td>190.48</td>
<td>0.635</td>
<td>0.046</td>
<td>0.120</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>265</td>
<td>93.32</td>
<td>20.26</td>
<td>0.980</td>
<td>283.98</td>
<td>0.702</td>
<td>0.038</td>
<td>0.120</td>
</tr>
<tr>
<td>120V</td>
<td>100</td>
<td>91.9</td>
<td>94.2</td>
<td>14.72</td>
<td>0.989</td>
<td>97.55</td>
<td>0.393</td>
<td>0.092</td>
<td>0.096</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>182</td>
<td>93.5</td>
<td>15.52</td>
<td>0.988</td>
<td>194.7</td>
<td>0.571</td>
<td>0.046</td>
<td>0.096</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>270</td>
<td>91.6</td>
<td>16.75</td>
<td>0.986</td>
<td>295.8</td>
<td>0.608</td>
<td>0.038</td>
<td>0.096</td>
</tr>
</tbody>
</table>

It can be observed from Table 10, that the efficiency, THD, and power factor of the proposed DCVM topology improve at lighter loads.

**Table 11: Simulation comparison between the proposed and the full bridge topology presented in [15]**

<table>
<thead>
<tr>
<th>V&lt;sub&gt;in&lt;/sub&gt; [Vrms]</th>
<th>P&lt;sub&gt;n&lt;/sub&gt; [W]</th>
<th>Efficiency [%]</th>
<th>THD [%]</th>
<th>PF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full bridge DCVM buck PFC</td>
<td>100</td>
<td>95.1</td>
<td>19.17</td>
<td>0.982</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>93.77</td>
<td>22.16</td>
<td>0.976</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>91.96</td>
<td>23.97</td>
<td>0.972</td>
</tr>
<tr>
<td>Proposed Bridgeless DCVM buck PFC</td>
<td>100</td>
<td>95.64</td>
<td>15.13</td>
<td>0.989</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>94.5</td>
<td>18.68</td>
<td>0.983</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>93.32</td>
<td>20.26</td>
<td>0.980</td>
</tr>
</tbody>
</table>
Fig. 5.20: Conversion ratio (M) versus duty cycle (D) at 100% & 95% Efficiency.
Chapter 6

Conclusions and Suggested Future Work

6.1 Conclusions

In this thesis, a new bridgeless step-down PFC converter topology operating in DCVM has been introduced. The harmonics' contents of the converter input current have been investigated. The efficiency of the converter has been compared with the full bridge PFC circuits. The proposed topology complies with the international standards, i.e. EN 61000-3-2. The new topology has been verified via PSpice simulation. It was concluded that:

1. The AC line input current of the proposed bridgeless PFC buck converter was in-phase with the input AC voltage. Hence, a power factor of 0.989, and efficiency of 95.64% have been achieved.
2. The input current harmonics have been reduced. The harmonics of the proposed DCVM topology satisfy the IEC 61000-3-2 limits, as shown in Fig. 5.2.
3. The DCVM operation offered additional advantages such as: zero-voltage turn-off at the power switches and zero-voltage turn-on at the output diode. As a result, the switching losses are reduced.
4. The two power switches ($Q_1$ and $Q_2$) are driven by one gating signal, which significantly simplifies the gating and control circuitry.
5. The load ground is non-floating with the input. This was achieved via return diodes $D_p$ and $D_n$. Hence, lower EMI was reached.
6. PSpice simulation has successfully verified the mathematical derivations of the topology.
7. The experimental results have successfully verified the simulated quantities and waveforms of the proposed topology.
Appendix A

The Simulation File (PSpice)

A.1 PSpice Simulation Code With real switches and diode models

The proposed topology was simulated using PSpice 16.3-p008, Cadence Design Systems Inc., as shown in Fig. A.1.

Fig. A.1: Simulated proposed topology with ideal components using PSpice.

Following are the instructions used to simulate the topology:

* Bridgeless PFC Buck Converter with DCVM Operation *
Vs 1 6 sin(0 141.42 50 0 0 0)
Vdc 1 2 dc 0V
L1 2 3 2.2m IC=0
L2 6 7 2.2m IC=0
C1 3 0 47n IC=0
C2 7 0 47n IC=0
Dp 0 6 DMOD
Do 0 4 DMOD
Lo 4 5 180u IC=0
Co 5 0 3000u IC=0
RL 5 0 23.04

*************************** Diode Model ***************************
* Model STTH5L06, 600V/5A/VF=0.85V @5A, Turbo2 Ultrafast High Voltage Rectifier
6.2 Suggestions for Future Work

The work in this thesis can be extended in different directions. Some of the ideas can be as follows:

1. Closed loop analysis and verifications.
2. The bridgeless buck DCVM topology can be extended to the Boost, Buck-Boost, Ćuk and other types of converter topologies.
A.2 PSpice Simulation Code All Real Components

E1 10 5 101 0 1
E2 11 5 102 0 1
E3 8 13 POLY(2) 6 8 6 12 0 0 0 0 0.115
G1 0 100 7 5 1u
D1 100 101 DID
D2 102 100 DID
R1 101 0 1MEG
R2 102 0 1MEG
.ENDS STY60NM60
.MODEL MOS NMOS (LEVEL=3 VTO=5.403 PHI=0.897 IS=0.1P + JS=0 THETA=0.108E-01 KP=44.869
.MODEL DGD D IS=0.1E-12 CJO=0.212E-10 VJ=0.779 M=0.311
.MODEL DBD D IS=0.1E-12 CJO=0.153E-09 VJ=0.748 M=0.217
.MODEL DBS D IS=0.1E-12 BV=644 N=1 TT=0.741E-06 RS=0.574E-01
.MODEL DID D IS=0.01E-12 RS=0 BV=654
*END OF MODELLING

******************** **************
.OPTIONS ITL2=200
.OPTIONS CHGTO L=10 n
.OPTIONS ITL5=0; *TOTAL ITERATION LIMIT
.OPTIONS LIMPTS=0; *MAXIMUM POINT ALLOWED
.OPTIONS ITL4=100; *ITERATION LIMIT PER POINT
.OPTIONS RELTOL=0.001; *REAL TOLERANCE
.OPTIONS VNTOL=1E-6
.OPTIONS NUMDGT=8
.OPTIONS ABSTOL=1E-6
.OPTIONS width=132

.TRAN 0.05u 400M 340M 0.05U uic
.PRINT TRAN i(vDC) v(5)
.FOUR 50 25 i(vDC) v(5)
.*.PROBE v(5) i(Vdc) i(Van) v(1,6) v(3,40)
.PROBE
.END
**Switch Section**

DQ1 40 4 DMOD
*M1 3 600 40 40 IXKK85N60C
X1 3 600 40 STY60NM60
Rg1 600 601 1
Eg1 601 40 51 0 12

DQ2 50 4 DMOD
*M2 7 700 50 50 IXKK85N60C
X2 7 700 50 STY60NM60
RG2 700 701 1
Eg2 701 50 51 0 12

*************** Gating Signals Multiplier ***************
Vg1 51 0 PULSE(0 1 0 5n 5n 9.67u 20u)
Vg2 53 0 PULSE(0 1 0 5n 5n 10m 20m)
Vg3 52 0 PULSE(0 1 10m 5n 5n 10m 20m)
EMULT2 55 0 VALUE = { V(51,0)*V(53,0) } 
EMULT1 54 0 VALUE = { V(51,0)*V(52,0) }

*************** Mosfet Model ***************
*XKK85N60C NMOS model 600V, 85A, 35mohm, Rg=2.2 Ohm
.MODEL IXKK85N60C NMOS (LEVEL=3 L=2.0000E-6 W=860
KP=1.0387E-6 RS=10.000E-3
+ RD=19.626E-3 VTO=3.4544 RDS=12.000E6 TOX=2.0000E-6
CGSO=11.628E-18 CGDO=729.90E-15
+ CBD=80.669E-9 MJ=1.1673 PB=3 RG=10.000E-3 IS=21.329E-6
N=2.3569 RB=1.0000E-9 GAMMA=0 KAPPA=0

* Modelling for STY60NM60 [RDS(on)=50 mohm, 600V, 60A,
RG=4.7 ohm]
.SUBCKT STY60NM60 1 2 3
LG 2 4 7.5E-9
LS 12 3 7.5E-9
LD 6 1 4.5E-9
RG 4 5 1.767
RS 9 12 0.446E-02
RD 7 6 0.204E-01
RJ 8 7 0.789E-02
CGS 5 9 0.636E-08
CGD 7 10 0.585E-08
CK 11 7 0.139E-09
DGD 11 7 DGD
DBS 12 6 DBS
DBD 9 7 DBD
MOS 13 5 9 9 MOS L=1u W=1u
Appendix B

Bode Plot Codes (Matlab)

B.1 Code of Bode Plot of the Line-to-Output Transfer Function

\[ D = 0.483; \]
\[ Dp = 1 - D; \]
\[ R = 23; \]
\[ Vg = 141.42; \]
\[ L1 = 2.2e^{-3}; \]
\[ Lo = 180e^{-6}; \]
\[ C1 = 47e^{-9}; \]
\[ Co = 3000e^{-6}; \]
\[ Ts = 20e^{-6}; \]
\[ Eff = 0.944; \]
\[ K = 2 \times R \times C1 / Ts; \]
\[ D1 = ((Eff \times K) / (2 \times Dp)) \times (1 + (sqrt(1 + ((4 \times Dp^2) / (Eff \times K))))) \]
\[ Vo = (D1 / (1 - D + D1)) \times Vg; \]
\[ I = Vo / R; \]
\[ num = (D1 / (1 - D + D1)); \]
\[ den = (((L1 \times Lo \times C1 \times Co) / ((1 - D + D1)^2)) \times (L1 \times Lo \times Co / (R \times (1 - D + D1)^2))) \]
\[ (((D1^2) \times L1 \times Co + L1 \times C1) / ((1 - D + D1)^2)) + Lo \times Co \]
\[ (((D1^2) \times L1 / (R \times (1 - D + D1)^2)) + Lo / R) \times 1; \]
\[ T = tf(num, den); \]
\[ freq = logspace(1, 5, 100); \]
\[ nn = length(freq); \]
\[ [mag_ratio, ph] = bode(T, freq); \]
\[ temp = 20 \times \log10(mag_ratio); \]
\[ mag_db = reshape(temp, [1 nn]); \]
\[ phase = reshape(ph, [1 nn]); \]
\[ subplot(211) \]
\[ semilogx(freq / (2 \times pi), mag_db); grid \]
\[ xlabel('Frequency (Hz)'); ylabel('Phase (deg)'); \]
\[ subplot(212) \]
\[ semilogx(freq / (2 \times pi), phase); grid \]
\[ xlabel('Frequency (Hz)'); ylabel('Phase (deg)'); \]
A real circuit is simulated using PSpice 16.3-p008, Cadence Design Systems Inc., as shown in Fig. A.2.

Fig. A.2: Simulated proposed topology with real components using PSpice.

Following are the instructions used to simulate the topology:

* Bridgeless Rectifier with DCVM Buck Converter (Real) *

** Topology 2 ****************************

Vs 1 6 sin(0 141.42 50 0 0 0)
Vdc 1 2 dc 0V
L1 2 110 2.2m IC=0
rl1 110 3 20m
L2 6 112 2.2m IC=0
rl2 112 7 20m
C1 3 113 47n IC=0
rc1 113 0 5m
C2 7 114 47n IC=0
rc2 114 0 5m
Dp 0 6 DMOD
Dn 0 2 DMOD
Do 0 4 DMOD
Lo 4 115 180u IC=0
rlo 115 5 10m
Co 5 116 3000u IC=0
rco 116 0 5m
RL 5 0 23.04
Appendix C

Derivations of the Formulae

C.1 Input Capacitor Voltage (Function of Time)

\[ v_{c1}(t) = \frac{I_1}{C_1} t - \frac{I_1}{C_1} DT_s \]  \hspace{1cm} (C.1)

\[ = \frac{I_1}{C_1} (t - DT_s) \]  \hspace{1cm} (C.2)

Substituting \((t = T_s)\) in eq. (C.2),

\[ V_{CM} = \frac{I_1}{C_1} (1 - D) T_s \]  \hspace{1cm} (C.3)

\[ V_{CM} = \frac{I_1}{C_1} D'T_s \]  \hspace{1cm} (C.4)

C.2 Averaged Input and Output Voltages

\( V_{in} \) equals the area of \( v_c \) as shown in Fig. 3.8,

\[ V_{in} = V_1 = \frac{1}{2} D_1 V_{CM} + \frac{1}{2} D_3 V_{CM} \]  \hspace{1cm} (C.5)

Also, \( D_3 \) can be found from the same Fig. 3.8,

\[ D_3 = 1 - D = D' \]  \hspace{1cm} (C.6)

Substituting \( D_3 \) in \( V_{in} \):

\[ V_1 = \frac{1}{2} (D' + D_1) V_{CM} \]  \hspace{1cm} (C.7)

The average voltage across the output inductor \( L_o \), over one switching cycle, is zero. Hence, the average output voltage \( V_o \) is equal to the average voltage across the input capacitor \( C_I \) only when the switch \( Q_I \) is closed.

Then,
B.2 Code of Bode Plot of the Control-to-Output Transfer Function

```plaintext
D=0.483;
Dp=1-D;
R=23;
Vg=141.42;
L1=2.2e-3;
Lo=180e-6;
C1=47e-9;
Co=3000e-6;
Ts=20e-6;
K=2*R*C1/Ts;
Eff=0.944;
D1=((Eff*K)/(2*Dp))*(1+(sqrt(1+((4*Dp^2)/(Eff*K)))))
Vc=Vg/(1-D+D1);
V=D1*Vc;
I=V/R;
I1=(D1/(1-D+D1))*I;
num=(D1/(1-D+D1))*((I1/(1-D+D1))+Vc);
den=[(L1*Lo*C1*Co/((1-D+D1)^2)) (L1*Lo*Co/(R*(1-D+D1)^2))]
(((D1^2)*L1*Co+L1*C1)/((1-D+D1)^2))+Lo*Co)
(((D1^2)*L1/(R*(1-D+D1)^2))+Lo/R) 1];
T=tf(num,den);
freq=logspace(1,6,100);
nn=length(freq);
[mag_ratio,ph]=bode(T,freq);
temp=20*log10(mag_ratio);
mag_db=reshape(temp,[1 nn]);
phase=reshape(ph,[1 nn]);
subplot(211)
semilogx(freq/(2*pi),mag_db);grid
xlabel('Frequency (Hz)');ylabel('Magnitude (dB)')
subplot(212)
semilogx(freq/(2*pi),phase);grid
xlabel('Frequency (Hz)');ylabel('Phase (deg)')
```

80
- First stage \((0 \leq t \leq DT_s)\):

\[ V_{L1} = V_m - V_{C1} \]  \hspace{1cm} (C.16)
\[ V_{L0} = V_{C1} - V_O \] \hspace{1cm} (C.17)
\[ I_{C1} = I_1 - I_2 \] \hspace{1cm} (C.18)
\[ I_{C0} = I_2 - I_O \] \hspace{1cm} (C.18)

- Second stage \((DT_s \leq t \leq T_s)\):

\[ V_{L1} = V_m - V_{C1} \] \hspace{1cm} (C.20)
\[ V_{L0} = -V_O \] \hspace{1cm} (C.21)
\[ I_{C1} = I_1 \] \hspace{1cm} (C.22)
\[ I_{C0} = I_2 - I_O \] \hspace{1cm} (C.23)

- The input inductor voltage \(\langle V_L(t) \rangle_{T_s}\) is zero over one switching cycle. Substituting eqs. (C.16) and (C.20) yields to:

\[ \langle V_{L1} \rangle_{T_s} = 0 \] \hspace{1cm} (C.24)
\[ V_{L1} DT_s + V_{L1} DT_s = 0 \] \hspace{1cm} (C.25)
\[ V_m = V_{C1} \] \hspace{1cm} (C.26)

- The output inductor voltage \(\langle V_{L0}(t) \rangle_{T_s}\) is zero over one switching cycle. Substituting eqs. (C.17) and (C.21) yields to:

\[ \langle V_{L0} \rangle_{T_s} = 0 \] \hspace{1cm} (C.27)
\[ V_{L0} DT_s + V_{L0} DT_s = 0 \] \hspace{1cm} (C.28)
\[ V_{C1} = \frac{V_O}{D} \] \hspace{1cm} (C.29)

- The charging current \(\langle i_{Cl}(t) \rangle_{T_s}\) through the input capacitor \(C_I\) is zero over one switching cycle. Substituting eqs. (C.18) and (C.22) yields to:
\[ V_0 = V_2 = \frac{1}{2} D_1 V_{CM} \]  

(C.8)

So, we can find the ratio between the output voltage to the input voltage by dividing \( V_2 \) by \( V_1 \),

\[
M = \left( \frac{V_2}{V_{in}} \right) = \left( \frac{V_2}{V_1} \right) = \frac{\frac{1}{2} D_1 V_{CM}}{\frac{1}{2} (1 - D + D_1) V_{CM}} = \frac{D_1}{1 - D + D_1} = \frac{D_1}{D' + D_1}
\]

(C.9)

\[ D_1 = (1 - D) \frac{V_2}{V_1 - V_2} = (1 - D) \frac{I_1}{I_2 - I_1} \]

(C.10)

Further simplification,

\[ \frac{V_2}{V_1 - V_2} = \frac{I_1}{I_2 - I_1} \]

(C.11)

Substituting eq. (C.4) in eq. (C.5):

\[ V_1 = \frac{1}{2} D_1 \left( \frac{I_1}{C_1} (1 - D) T_s \right) + \frac{1}{2} \left( \frac{I_1}{C_1} (1 - D)^2 T_s \right) \]

(C.12)

\[ \langle v_1(t) \rangle = V_1 = \frac{I_1}{2 C_1} - T_s D' (D' + D_1) \]

(C.13)

\[ V_2 \] can be written after substituting eq. (C.4) in eq. (C.8) as follows,

\[ V_2 = \frac{I_1}{2 C_1} T_s (1 - D) D_1 \]

(C.14)

\[ \langle v_2(t) \rangle = V_2 = \frac{I_1}{2 C_1} T_s D' D_1 \]

(C.15)

C.3 Large-Signal Analysis during CCVM

There are two stages during CCVM. The charging current \( \langle i_C(t) \rangle_{T_s} \) through the input capacitor \( C_1 \) is zero over one switching cycle \( T_s \). Also, the inductors' voltages \( \langle v_L(t) \rangle_{T_s} \) are zero over \( T_s \) as follows,
\( I_{C_1} = 0 \)  \\
\( I_{C_o} = I_2 - I_O \)  \( \text{(C.44)} \)  \( \text{(C.45)} \)

- Third stage \((DT_s \leq t \leq T_s)\):

\( V_{L1} = V_m - V_{C1} \)  \( \text{(C.46)} \)

\( V_{L0} = -V_O \)  \( \text{(C.47)} \)

\( I_{C1} = I_1 \)  \( \text{(C.48)} \)

\( I_{C0} = I_2 - I_O \)  \( \text{(C.49)} \)

- The input inductor voltage \( \langle v_{L1}(t) \rangle_{T_s} \) is zero over one switching cycle. Substituting eqs. (C.37), (C.41) and (C.46) yields to:

\[ \langle V_{L1} \rangle_{T_s} = 0 \]  \( \text{(C.50)} \)

\[ V_{L1} D_1 T_s + V_{L1} D_2 T_s + V_{L1} D_3 T_s = 0 \]  \( \text{(C.51)} \)

\[ V_{C1} = \frac{V_m}{D_1 + D'} \]  \( \text{(C.52)} \)

- The output inductor voltage \( \langle v_{L0}(t) \rangle_{T_s} \) is zero over one switching cycle. Substituting eqs. (C.38), (C.43) and (C.47) yields to:

\[ \langle V_{L0} \rangle_{T_s} = 0 \]  \( \text{(C.53)} \)

\[ V_{L0} D_1 T_s + V_{L0} D_2 T_s + V_{L0} D_3 T_s = 0 \]  \( \text{(C.54)} \)

\[ V_{C1} = \frac{V_o}{D} \]  \( \text{(C.55)} \)

- The charging current \( \langle i_{C1}(t) \rangle_{T_s} \) through the input capacitor \( C_I \) is zero over one switching cycle. Substituting eqs. (C.39), (C.44) and (C.48) yields to:

\[ \langle I_{C1} \rangle_{T_s} = 0 \]  \( \text{(C.56)} \)

\[ I_{C1} D_1 T_s + I_{C1} D_2 T_s + I_{C1} D_3 T_s = 0 \]  \( \text{(C.57)} \)
\(\langle I_{c1} = 0 \rangle_{T_S}\)  \quad \text{(C.30)}
\[ I_{c1} D T_S + I_{c1} D' T_S = 0 \]  \quad \text{(C.31)}
\[ I_1 = D I_2 \]  \quad \text{(C.32)}

This yield to,
\[ I_{c1} = I_1 - D I_2 \]  \quad \text{(C.33)}

- The charging current \(\langle i_{c_o}(t) \rangle\) through the output capacitor \(C_o\) is zero over one switching cycle. Substituting eqs. (C.19) and (C.23) yields to:
\[ \langle I_{c_o} = 0 \rangle_{T_S} \]  \quad \text{(C.34)}
\[ I_{c_o} D T_S + I_{c_o} D' T_S = 0 \]  \quad \text{(C.35)}
\[ I_2 = I_0 \]  \quad \text{(C.36)}

\subsection*{C.4 Large-Signal Analysis during DCVM}

There are three stages during DCVM. The charging current \(\langle i_c(t) \rangle_{T_S}\) through the input capacitor \(C_i\) is zero over one switching cycle \(T_s\). Also, the inductors' voltages \(\langle V_L(t) \rangle\) are zero over \(T_s\). This is shown in the following equations:

- First stage \((0 \leq t \leq D_1 T_s)\):
\[ V_{L1} = V_m - V_{C1} \]  \quad \text{(C.37)}
\[ V_{L0} = V_{C1} - V_o \]  \quad \text{(C.38)}
\[ I_{C1} = I_1 - I_2 \]  \quad \text{(C.39)}
\[ I_{C0} = I_2 - I_0 \]  \quad \text{(C.40)}

- Second stage \((D_1 T_s \leq t \leq DT_s)\):
\[ V_{L1} = V_m \]  \quad \text{(C.41)}
\[ V_{C1} = 0 \]  \quad \text{(C.42)}
\[ V_{L0} = -V_o \]  \quad \text{(C.43)}
\[ V_o = \frac{I_1}{2C_1} T_s D' D_1 + D_1 V_{c1} \quad \text{(C.67)} \]

The boundary condition between DCVM and CCVM is when \( D_1 = D \),

\[ V_o = \frac{I_1}{2C_1} T_s D' D + D V_{c1} \quad \text{(C.68)} \]

### C.6 Effective Input Resistance

From eq. (C.9),

\[ D_1 + D' = D_1 \left( \frac{V_m}{V_o} \right) , \text{ and} \quad \text{(C.69)} \]

\[ D_1 = D' \left( \frac{V_o}{V_m - V_o} \right) \quad \text{(C.70)} \]

Dividing \( V_{in} \) in eq. (C.13) by \( I_{in} \),

\[ R_{r\text{-eff}} = \frac{V_m}{I_m} = \frac{T_s}{2C_1} D' (D' + D_1) \quad \text{(C.71)} \]

\[ R_{r\text{-eff}} = \frac{T_s}{2C_1} D' D_1 \left( \frac{V_m}{V_o} \right) \quad \text{(C.72)} \]

\[ R_{r\text{-eff}} = \frac{T_s}{2C_1} D^2 \left( \frac{V_o}{V_m - V_o} \right) \left( \frac{V_m}{V_o} \right) \quad \text{(C.73)} \]

\[ R_{r\text{-eff}} = \frac{V_i}{I_i} = \frac{D^2 T_s}{2C_1} \left( \frac{V_i}{V_i - V_o} \right) \quad \text{(C.74)} \]

### C.7 Input Energy Over Half-Line Cycle

Substituting eq. (3.33) and eq. (3.34) in eq. (3.36),

\[ E_i = \int_{0}^{T/2} v_i(t) i_i(t) \, dt = \int_{0}^{T/2} V_i \sin \left( \frac{2\pi}{T_c} t \right) \cdot \frac{2C_1 V_i}{T_s D^2} \left( \sin \left( \frac{2\pi}{T_c} t \right) - M \right) \, dt \quad \text{(C.75)} \]
\[ I_{C1} = I_1(D'+D_i) = D_i I_2 \]  

(C.58)

- The charging current \( \langle i_{C_o}(t) \rangle_{T_s} \) through the output capacitor \( C_o \) is zero over one switching cycle. Substituting eqs. (C.40), (C.45) and (C.49) yields to:

\[
\langle I_{C_o} = 0 \rangle_{T_s} = 0 \]  

(C.59)

\[ I_{C_o} D_1 T_s + I_{C_o} D_2 T_s + I_{C_o} D_3 T_s = 0 \]  

(C.60)

\[ I_2 = I_o \]  

(C.61)

C.5 Averaged Steady-State for DCVM & CCVM (Input and Output Voltages)

1. From the input circuit of Fig. 3.12 we can find the voltage loop equation as follows:

\[ V_{in} = V_1 + V_{C1}(D'+D_i) \]  

(C.62)

Substituting eq. (C.13),

\[ V_{in} = \frac{I_1}{2 C_1} T_s D'(D'+D_i) + V_{C1}(D'+D_i) \]  

(C.63)

The boundary condition between DCVM and CCVM is when \( D_f = D \),

\[ V_{in} = \frac{I_1}{2 C_1} T_s D'(D'+D) + V_{C1}(D'+D) \]  

(C.64)

But \( D'+D=I \), then,

\[ V_{in} = \frac{I_1}{2 C_1} T_s D' + V_{C1} \]  

(C.65)

2. From the output circuit Fig. 3.12 we can find the voltage loop equation as follows:

\[ V_o = V_2 + D_1 V_{C1} \]  

(C.66)

Substituting eq. (C.15),
\[ \eta = \frac{2 D'^2}{K} \left( \frac{\pi V_0^2}{\pi V_i^2 - 4 V_i V_0} \right) \]  

(C.83)

Solving for \( \frac{V_0}{V_i} \),

\[ \frac{V_0}{V_i} = 0 \]

(C.84)

\[ \frac{V_0}{V_i} = -\frac{\eta K}{2 D'^2} + \sqrt{\frac{\eta^2 K^2}{\pi^2 D'^4} + \frac{\eta K}{2 D'^2}} = -\frac{\eta K}{2 D'^2} + \sqrt{\frac{\eta^2 K^2}{\pi^2 D'^4} \left( 1 + \frac{\pi^2 D'^2}{2 \eta K} \right)} \]  

(C.85)

\[ \frac{V_0}{V_i} = -\frac{\eta K}{2 D'^2} + \frac{\eta K}{\pi D'^2} \sqrt{1 + \frac{\pi^2 D'^2}{2 \eta K}} \]  

(C.86)

\[ M = \frac{\eta K}{\pi D'^2} \left( \sqrt{1 + \frac{\pi^2 D'^2}{2 \eta K}} - 1 \right) \]  

(C.87)

C.9 Normalized Discharging Time

From eq. (C.15),

\[ I_1 = \frac{2 C_1}{T_s D' D_1} V_2 \]  

(C.88)

Substituting \( I_1 \) and \( I_2 \) in \( \eta \),

\[ \eta = \frac{I_2}{I_1} \left( \frac{D_1}{D' + D_1} \right) \]  

(C.89)

Then,

\[ \eta = \frac{T_s}{2 C_1 R_L} D' \left( \frac{D_1^2}{D' + D_1} \right) \]  

(C.90)

Substituting eq. (3.41),

\[ D' D_1^2 = \eta K D' + \eta K D_1 \]  

(C.91)
\[ T_{c/2} = \int_{0}^{T_{c/2}} 2C_{1}V_{i}^2 \left( \sin^2 (\omega_{L} t) - M \sin (\omega_{L} t) \right) \, dt \]  

(C.76)

Where \( \omega_{L} = \frac{2\pi}{T_{L}} \).

Let \( J = \frac{2C_{1}V_{i}^2}{T_{S}D^2} \)

\[ T_{c/2} = \left[ \frac{J}{2} - \frac{J}{4\omega_{L}} \sin (2\omega_{L} t) + \frac{JM}{\omega_{L}} \cos (\omega_{L} t) \right]_{0}^{T_{c/2}} \]  

(C.77)

\[ T_{c/2} = \frac{JT_{L}}{2} - \frac{JM}{4\omega_{L}} \sin \left( 2\omega_{L} \frac{T_{L}}{2} \right) + \frac{JM}{\omega_{L}} \cos \left( \frac{T_{L}}{2} \right) - \frac{JM}{\omega_{L}} \cos (0) \]  

(C.78)

\[ T_{c/2} = \frac{JT_{L}}{2} - \frac{JM}{\omega_{L}} \frac{J}{\omega_{L}} = \frac{JT_{L}}{2} - \frac{2JM}{\omega_{L}} \]  

(C.79)

\[ E_{i} = \frac{C_{1}T_{L}}{2T_{S}D^2} \left( V_{i}^2 - \frac{4V_{i}V_{o}}{\pi} \right) \]  

(C.80)

### C.8 Voltage Conversion “Gain” Ratio in DCVM

Substituting eqs. (3.37) and (3.38) in eq. (3.39) we get,

\[ \eta = \frac{P_{o}}{P_{in}} \quad \text{(C.81)} \]

However, the efficiency \( \eta \) can be found from the relationship between the input energy \( E_{i} \) and the output energy \( E_{o} \) as follows:

\[ \eta = \frac{V_{o}^2T_{L}}{2R_{L}} = \frac{2T_{S}D^2}{C_{1}R_{L}} \left( \frac{V_{o}^2}{V_{i}^2 - \frac{4V_{i}V_{o}}{\pi}} \right) \]  

(C.82)

Substituting eq. (3.41),
\[ D = \frac{\eta K_{Cr}}{2D'} \left( 1 + \sqrt{1 + \frac{4D'^2}{\eta K_{Cr}}} \right) \]  
\[ \frac{2D'D}{\eta K_{Cr}} - 1 = \sqrt{1 + \frac{4D'^2}{\eta K_{Cr}}} \]  
\[ \frac{4D'^2}{\eta^2 K_{Cr}} - \frac{4D'D}{\eta^2 K_{Cr}} + 1 = \frac{4D'^2}{\eta K_{Cr}} \]  
Multiplying by \( \frac{\eta^2 K_{Cr}^2}{4D'} \) yields to:  
\[ \frac{D^2D'}{\eta} - D K_{Cr} - D' K_{Cr} = 0 \]  
But \( D + D' = 1 \), then:  
\[ K_{Cr} = \frac{D^2D'}{\eta} \]  

**C.12 Input rms current**

Solving for \( I_{(rms)} \) from eq. (3.34),

\[ I_{(rms)} = \sqrt{\frac{2}{T_L} \int_0^{T_L/2} t^2 dt} = \sqrt{\frac{2}{T_L} \int_0^{T_L/2} \left( \frac{2C_L V_s}{T_S D'} \right)^2 \left( \sin(\omega_L t) - M \right)^2 dt} \]  
Let \( J = \frac{2C_L V_s}{T_S D'} \), then,

\[ I_{(rms)} = \sqrt{\frac{2J^2 T_L}{T_S} \int_0^{T_L/2} \left( \sin^2(\omega_L t) - 2M \sin(\omega_L t) + M^2 \right) dt} \]  

\[ = \sqrt{\frac{2J^2}{T_L} \left( \frac{t}{2} - \frac{\sin(2\omega_L t)}{4\omega_L} + \frac{2M}{\omega_L} \cos(\omega_L t) + M^2 t \right) \left( \frac{t}{2} \right)^{T_L/2}} = \sqrt{\frac{2J^2}{T_L} \left( \frac{T_L}{4} - \frac{2M}{\omega_L} \right) \left( \frac{M^2 T_L}{2} - \frac{2M}{\omega_L} \right)} \]
\[ D_1^2 - \frac{\eta K}{D'} D_1 - \eta K = 0 \]  

(C.92)

Using the quadratic formula,

\[ D_1 = \frac{\eta K}{2D'} \pm \sqrt{\left(\frac{\eta K}{2D'} \right)^2 + \eta K} \]  

(C.93)

Solving for \( D_1 \) with the ignorance of the negative sign in the normalized discharge time formula,

\[ D_1 = \frac{\eta K}{2D'} \left(1 + \frac{4D'^2}{\eta K}\right) \]  

(C.94)

\[ D_1 = \frac{\eta K}{2D'} \left(1 + \sqrt{\frac{4D'^2}{\eta K}}\right) \]  

(C.95)

\section*{C.10 Normalized Discharging Time (Function of Time)}

Solving eq. (C.9) for \( D_1 \),

\[ D_1 = D' \left(\frac{V_o}{V_i - V_o}\right) \]  

(C.96)

Solving for the time variant function of \( d_1(t) \),

\[ d_1(t) = D' \left(\frac{V_o}{V_i \sin(\omega_i t) - V_o}\right) \]  

(C.97)

\[ d_1(t) = D' \left(\frac{M}{\sin(\omega_i t) - M}\right) \]  

(C.98)

\section*{C.11 \( K_{\text{Ccre}} \) for Boundary Condition Between CCVM & DCVM}

Considering the boundary condition \( D_1 = D \), then eq. (C.95) will be,
\[
\langle v_{i0} \rangle_{I_{i}} = L_{0} \frac{d}{dt} \langle i_{2} \rangle_{I_{i}} = d_{1}(t)\left[\langle v_{c} \rangle_{I_{i}} - \langle v_{0} \rangle_{I_{i}} \right] + d_{3}(t)\left[ -\langle v_{0} \rangle_{I_{i}} \right] - d_{1}(t)\langle v_{0} \rangle_{I_{i}}
\]

(C.113)

Simplifying the equation yields to,
\[
\langle v_{i0} \rangle_{I_{i}} = d_{1}(t)\langle v_{c} \rangle_{I_{i}} - \langle v_{0} \rangle_{I_{i}}
\]

(C.114)

**C.17  Averaging Input Capacitor**

Substituting (3.64), (3.68) and (3.72), we get:
\[
\langle i_{c1} \rangle_{I_{i}} = C_{1} \frac{d}{dt} \langle v_{c} \rangle_{I_{i}} = d_{1}(t)\left[\langle i_{1} \rangle - \langle i_{2} \rangle \right] + d_{2}(t)\left[0\right] + d_{3}(t)\left[\langle i_{i} \rangle \right]
\]

(C.115)

Simplifying the equation yields to,
\[
\langle i_{c1} \rangle_{I_{i}} = C_{1} \frac{d}{dt} \langle v_{c} \rangle_{I_{i}} = \langle i_{i} \rangle - \langle i_{2} \rangle + d_{1}(t)\left[\langle i_{i} \rangle \right]
\]

(C.116)

**C.18  Averaging Output Capacitor**

Substituting (3.65), (3.69) and (3.73), we get:
\[
\langle i_{o} \rangle_{I_{i}} = C_{0} \frac{d}{dt} \langle v_{o} \rangle_{I_{i}} = d_{1}(t)\left[\langle i_{2} \rangle - \langle v_{0} \rangle \right] + d_{2}(t)\left[\langle i_{2} \rangle - \langle v_{0} \rangle \right] + d_{3}(t)\left[\langle i_{2} \rangle - \langle v_{0} \rangle \right]
\]

\[
+ d_{1}(t)\left[\langle i_{2} \rangle - \langle v_{0} \rangle \right] + d_{1}(t)\left[\langle i_{2} \rangle - \langle v_{0} \rangle \right]
\]

(C.117)

Simplifying the above equation yields to,
\[
\langle i_{o} \rangle_{I_{i}} = C_{0} \frac{d}{dt} \langle v_{o} \rangle_{I_{i}} = \langle i_{2} \rangle - \langle v_{0} \rangle
\]

(C.118)

**C.19  Linearization of the Input Inductor**

Substituting eqs. of (3.78) in to the nonlinear equation (3.74),
\[
L_{1} \left[ \frac{d}{dt} I_{1} + \frac{d}{dt} \hat{I}_{1}(t) \right] = [V_{1} + \hat{V}_{i}(t) - (V_{c} + \hat{V}_{c}(t))\left[1 - (D + \hat{d}(t)) + (D_{1} + \hat{d}_{1}(t)) \right]
\]

(C.119)
\[ I_{l rms} = \frac{C_1 V_i}{T_s D_2^2} \left( 2 - \frac{16}{\pi} M + 4M^2 \right) \]  
(C.107)

C.13 Average Input Power

Solving the average input power over one-half cycle using eq. (C.80),

\[ P_{in} = \frac{2}{T_L} E_i = \frac{2}{T_L} \frac{C_1 T_L}{2 T_s D^2} \left( V_{i}^2 - \frac{4V_I V_Q}{\pi} \right) = \frac{C_1 V_i^2}{T_s D_2^2} \left( 1 - \frac{4}{\pi} M \right) \]  
(C.108)

C.14 Converter's Power Factor

Substituting eqs. (3.47) and (3.48) in eq. (3.46) yields to,

\[ P_F = \frac{\frac{C_1 V_i^2}{T_s D_2^2} \left( 1 - \frac{4}{\pi} M \right)}{\sqrt{2} \frac{C_1 V_i^2}{T_s D_2^2} \left( 2 - \frac{16}{\pi} M + 4M^2 \right)} = \frac{1 - \frac{4}{\pi} M}{\sqrt{1 - \frac{8}{\pi} M + 2M^2}} \]  
(C.109)

C.15 Averaging Input Inductor

Substituting eqs. (3.62), (3.66) and (3.70), we get:

\[ \langle v_{L_1} (t) \rangle_{T_S} = L_1 \frac{d \langle i_1 (t) \rangle_{T_S}}{dt} = d_1 (t) \left[ \langle v_1 (t) \rangle_{T_S} - \langle v_C (t) \rangle_{T_S} \right] + d_2 (t) \left[ \langle v_1 (t) \rangle_{T_S} - \langle v_C (t) \rangle_{T_S} \right] + d_3 (t) \left[ \langle v_1 (t) \rangle_{T_S} - \langle v_C (t) \rangle_{T_S} \right] \]  
(C.110)

Simplifying the equation yields to,

\[ \langle v_{L_1} (t) \rangle_{T_S} = \langle v_1 (t) \rangle_{T_S} - \langle v_C (t) \rangle_{T_S} \left[ d_1 (t) + d_2 (t) \right] \]  
(C.111)

Where, \( d_3 (t) = 1 - d(t) \)

Then,

\[ \langle v_{L_1} (t) \rangle_{T_S} = L_1 \frac{d \langle i_1 (t) \rangle_{T_S}}{dt} = \langle v_1 (t) \rangle_{T_S} - \langle v_C (t) \rangle_{T_S} \left[ 1 - d(t) + d_1 (t) \right] \]  
(C.112)

C.16 Averaging Output Inductor

Substituting eqs. (3.63), (3.67) and (3.71), we get:
The nonlinear 2\textsuperscript{nd} order AC term is ignored, since it is very small compared to the DC components and to the 1\textsuperscript{st} order terms. Also, the 2\textsuperscript{nd} order AC terms contain the product of AC quantities, which makes them nonlinear because they involve the multiplication of time-varying signals. Therefore, the above equation is expressed as,

\begin{equation}
L_o \frac{d^2 i_2(t)}{d t^2} = D_1 V_C - V_o + D_1 \dot{V}_C(t) + \dot{d}_1(t)V_C - \ddot{V}_o(t)
\end{equation}

The resulting DC terms are

\begin{equation}
D_1 V_C - V_o = 0
\end{equation}

The 1\textsuperscript{st} order AC terms (linear) are

\begin{equation}
L_o \frac{d \dot{i}_2(t)}{d t} = D_1 \dot{V}_C(t) + \dot{d}_1(t)V_C - \ddot{V}_o(t)
\end{equation}

C.21 Linearization of the Input Capacitor

Substituting eqs. (3.78) into the nonlinear equation (3.76),

\begin{equation}
C_1 \left[ \frac{d V_C}{d t} + \frac{d \dot{V}_C(t)}{d t} \right] = (I_1 + i(t))\left[ - (D + \dot{d}(t)) + (D_1 + \dot{d}_1(t)) \right] - (D_1 + \dot{d}_1(t))I_2 + \dot{i}_2(t))
\end{equation}

where

\begin{equation}
C_1 \frac{d V_C}{d t} = 0
\end{equation}

Rearranging the equation yields

\begin{equation}
C_1 \left[ 0 + \frac{d \dot{V}_C(t)}{d t} \right] = I_1 (1 - D + D_1) - D_1 I_2 + \left[ \dot{d}_1(t) - \dot{d}(t) \right] I_1 + (1 - D + D_1) \dot{i}_1(t) - D_1 \dot{i}_1(t) \dot{I}_2(t) + \dot{d}_1(t) \dot{i}_2(t)
\end{equation}

The nonlinear 2\textsuperscript{nd} order AC terms are ignored, since they are very small compared to the DC components and to the 1\textsuperscript{st} order terms. Also, the 2\textsuperscript{nd} order AC terms contain the product of AC quantities, which makes them nonlinear because they involve the multiplication of time-varying signals. So, the above equation can be presented as,

\begin{equation}
C_1 \frac{d \dot{V}_C(t)}{d t} = I_1 (1 - D + D_1) - D_1 I_2 + \left[ \dot{d}_1(t) - \dot{d}(t) \right] I_1 + (1 - D + D_1) \dot{i}_1(t) - D_1 \dot{i}_1(t) \dot{I}_2(t) - \dot{d}_1(t) I_2
\end{equation}
where \( L_1 \frac{d I_1}{dt} = 0 \)

Rearranging the equation yields

\[
L_1 \left[ 0 + \frac{d i_1(t)}{dt} \right] = V_1 - (1 - D + D_1) V_C + \hat{v}_c(t) - (1 - D + D_1) \hat{v}_c(t) - \left[ \hat{a}_1(t) - \hat{a}(t) \right] \hat{\gamma}_c(t)
\]

(C.120)

The nonlinear 2nd order AC terms are ignored, since they are very small compared to the DC components and to the 1st order AC terms. Also, the 2nd order AC terms contain the product of as quantities, which makes them nonlinear because they involve the multiplication of time-varying signals. Therefore, the above equation can be written as

\[
L_1 \frac{d i_1(t)}{dt} = V_1 - (1 - D + D_1) V_C + \hat{v}_c(t) - (1 - D + D_1) \hat{v}_c(t) - \left[ \hat{a}_1(t) - \hat{a}(t) \right] \hat{\gamma}_c(t)
\]

(C.121)

The resulting DC terms are

\[ V_1 - (1 - D + D_1) V_C = 0 \]

(C.122)

The 1st order AC terms (linear) are

\[
L_1 \frac{d i_1(t)}{dt} = \hat{v}_c(t) - (1 - D + D_1) \hat{v}_c(t) + \left[ \hat{a}(t) - \hat{a}_1(t) \right] \hat{\gamma}_c(t)
\]

(C.123)

### C.20 Linearization of the Output Inductor

Substituting eqs. of (3.78) in to the nonlinear equation (3.75),

\[
L_o \left[ \frac{d I_2}{dt} + \frac{d \hat{i}_2(t)}{dt} \right] = (D_1 + \hat{d}_1(t))(V_C + \hat{v}_c(t)) - (V_O + \hat{v}_o(t))
\]

(C.124)

where \( L_o \frac{d I_2}{dt} = 0 \)

Rearranging the equation yields

\[
L_o \left[ 0 + \frac{d \hat{i}_2(t)}{dt} \right] = D_1 V_C - V_O + D_1 \hat{v}_c(t) + \hat{d}_1(t) V_C - \hat{v}_o(t) + \hat{d}_1(t) \hat{v}_c(t)
\]

(C.125)
\[ \hat{v}_o(s) = \hat{v}_c(s) \frac{\left( \frac{R_L}{sC_o} \right)}{sL_c + \left( \frac{R_L}{sC_o} \right)} \]  

(C.138)

Solving for \( \hat{v}_o(s) \):

\[ \hat{v}_o(s) = \frac{1}{s^2 L_o C_o + s \frac{L_o}{R_L} + 1} \hat{v}_c(s) \]  

(C.139)

Then, solving the above equation for \( \hat{v}_c(s) \),

\[ \hat{v}_c(s) = \left( s^2 L_o C_o + s \frac{L_o}{R_L} + 1 \right) \hat{v}_o(s) \]  

(C.140)

Simplifying the equivalent circuit of Fig. 3.25(c) gives the equivalent circuit of Fig. 3.26,

\[ Z_{eq} = \left( sL_o + \left( \frac{R_L}{sC_o} \right) \right) / \left( \frac{D^2}{sC_1} \right) \]  

(C.141)

Extract \( sL_o + \left( \frac{R_L}{sC_o} \right) \),

\[ \left( sL_o + \left( \frac{R_L}{sC_o} \right) \right) = sL_o + \left( \frac{R_L}{1 + sR_L C_o} \right) = \frac{s^2 R_L L_o C_o + sL_o + R_L}{1 + sR_L C_o} \]  

(C.142)

\[ Z_{eq} = \left( \frac{s^2 L_o C_o + s \frac{L_o}{R_L} + 1}{sC_o + \frac{1}{R_L}} \right) / \left( \frac{D^2}{sC_1} \right) \]  

(C.143)

After further manipulations, the above equation yields
The resulting DC terms are

\[ I_1 (1-D+D_1) - D_1 I_2 = 0 \]  \hspace{1cm} (C.132)

The linearized 1st order AC terms are

\[ C_1 \frac{d \hat{v}_c(t)}{dt} = -\dot{a}(t) I_1 + \hat{a}_1(t)(I_1 - I_2) + (1-D+D_1)\hat{i}_1(t) - D_1 \hat{i}_2(t) \]  \hspace{1cm} (C.133)

### C.22 Linearization of the Output Capacitor

Substituting eqs. (3.78) into the nonlinear equation (3.77),

\[
C_o \left[ \frac{dV_o}{dt} + \frac{d\hat{V}_o(t)}{dt} \right] = \left( I_2 + \hat{i}_2(t) \right) - \frac{\left( V_o + \hat{V}_o(t) \right)}{R_L}
\]  \hspace{1cm} (C.134)

Where, \( C_o \frac{dV_o}{dt} = 0 \)

Rearranging the equation yields

\[
C_o \frac{d\hat{V}_o(t)}{dt} = I_2 - \frac{V_o}{R_L} + \hat{i}_2(t) - \frac{\hat{V}_o(t)}{R_L}
\]  \hspace{1cm} (C.135)

The resulting DC terms are

\[ I_2 - \frac{V_o}{R_L} = 0 \]  \hspace{1cm} (C.136)

The linearized 1st order AC terms are

\[
C_o \frac{d\hat{V}_o(t)}{dt} = \hat{i}_2(t) - \frac{\hat{V}_o(t)}{R_L}
\]  \hspace{1cm} (C.137)

### C.23 Line-to-Output Transfer Function

Applying the voltage divider technique to find the relation between \( \hat{v}_c(s) \) and \( \hat{v}_c(s) \), in Fig. 3.25(c),
Control-to-Output Transfer Function ( dependent current source deactivated)

The voltage divider technique is applied to find the relation between $\hat{v}_o(s)$ and $\hat{v}_e(s)$,

$$\hat{v}_o(s) = \hat{v}_e(s) \frac{\left( R_L \parallel \frac{1}{sC_o} \right)}{sL_o + \left( R_L \parallel \frac{1}{sC_o} \right)}$$ (C.150)

Normalizing the above equation, and solving for $\hat{v}_e(s)$,

$$\hat{v}_e(s) = \left( s^2 L_o C_o + \frac{L_o}{R_L} + 1 \right) \hat{v}_o(s)$$ (C.151)

$$Z_{eq} = \left( sL_o + \left( R_L \parallel \frac{1}{sC_o} \right) \right) \parallel \frac{D_1^2}{sC_1}$$ (C.152)

Solving for $\left( sL_o + \left( R_L \parallel \frac{1}{sC_o} \right) \right)$,

$$\left( sL_o + \left( R_L \parallel \frac{1}{sC_o} \right) \right) = sL_o + \left( \frac{R_L}{1 + sR_L C_o} \right) = \frac{s^2 R_L L_o C_o + sL_o + R_L}{1 + sR_L C_o}$$ (C.153)

and substitute the above equation in eq. (3.91),

$$Z_{eq} = \frac{\left( s^2 L_o C_o + \frac{L_o}{R_L} + 1 \right)}{sC_o + \frac{1}{R_L}} \parallel \frac{D_1^2}{sC_1}$$ (C.154)

Simplifying the above equation,

$$Z_{eq} = \frac{D_1^2 \left( s^2 L_o C_o + \frac{L_o}{R_L} + 1 \right)}{s^3 L_o C_1 C_o + s^2 \frac{L_o C_1}{R_L} + s \left( D_1^2 C_o + C_1 \right) + \frac{D_1^2}{R_L}}$$ (C.155)
The voltage divider technique is applied to find the relation between $\hat{v}_1(s)$ and $\hat{v}_c(s)$.

$$
\hat{v}_c(s) = \hat{v}_1(s) \frac{\left( \frac{D_1}{1 - D + D_1} \right) * Z_{eq}}{Z_{eq} + \left( \frac{D_1}{1 - D + D_1} \right)^2 s L_1}
$$

Substitution of $\hat{v}_c(s)$ yields

$$
\left( s^2 L_c C_o + s \frac{L_o}{R_L} + 1 \right) \hat{v}_c(s) = \hat{v}_1(s) \frac{\left( \frac{D_1}{1 - D + D_1} \right) * Z_{eq}}{Z_{eq} + \left( \frac{D_1}{1 - D + D_1} \right)^2 s L_1}
$$

The expression for $\frac{\hat{v}_c(s)}{\hat{v}_1(s)}$ becomes

$$
\frac{\hat{v}_c(s)}{\hat{v}_1(s)} = \frac{D_1 (1 - D + D_1)}{(1 - D + D_1)^2 \left( s^2 L_c C_o + s \frac{L_o}{R_L} + 1 \right) + s^4 L_4 L_c C_4 C_o + s^3 \frac{L_o C_1}{R_L} + s^2 \left( D_1^2 L_c C_o + L_c C_1 \right) + s \frac{D_1^2 L_c}{R_L}}
$$

Finally, normalizing the above equation yields

$$
G_{eq}(s) = \frac{\hat{v}_c(s)}{\hat{v}_1(s) \hat{v}_1(s)} = \frac{\left( \frac{D_1}{1 - D + D_1} \right)}{s^4 \frac{L_c C_o R_L}{(1 - D + D_1)^2} + s^2 \frac{L_c C_o}{R_L (1 - D + D_1)^2} + s^2 \frac{D_1^2 L_c C_o + L_c C_1}{R_L (1 - D + D_1)^2} + s \frac{D_1^2 L_c}{R_L (1 - D + D_1)^2} + s \frac{L_o}{R_L} + 1}
$$
\[ \hat{v}_o(s) = \hat{v}_e(s) \frac{1}{s^2L_0C_o + s \frac{L_o}{R_L} + 1} \]  
(C.161)

Solving the above equation for \( \hat{v}_e(s) \),

\[ Z_{eq} = \left( sL_o + \left( R_L // \frac{1}{sC_o} \right) \right) \left/ \frac{D_i^2}{sC_1} \right. \]  
(C.162)

Find \( sL_o + \left( R_L // \frac{1}{sC_o} \right) \),

\[ \left( sL_o + \left( R_L // \frac{1}{sC_o} \right) \right) = sL_o + \left( \frac{R_L}{1 + sR_LC_o} \right) = \frac{s^2R_LL_oC_o + sL_o + R_L}{1 + sR_LC_o} \]  
(C.163)

Then, substitute the above equation in eq. (3.93),

\[ Z_{eq} = \left( \frac{s^2L_0C_o + s \frac{L_o}{R_L} + 1}{sC_o + \frac{1}{R_L}} \right) \left/ \frac{D_i^2}{sC_1} \right. \]  
(C.164)

Simplifying the above equation,

\[ Z_{eq} = \frac{D_i^2 \left( s^2L_0C_o + s \frac{L_o}{R_L} + 1 \right)}{s^3L_oC_1C_o + s^2 \frac{L_o}{R_L} + s \left( D_i^2C_o + C_1 \right) + \frac{D_i^2}{R_L}} \]  
(C.165)

Apply the voltage divider technique to find the relation between \( \hat{d}(s) \) and \( \hat{v}_e(s) \),

\[ \hat{v}_e(s) = \hat{d}(s) \left( \frac{D_i}{(1 - D + D_i)^2} \right) L_1 * Z_{eq} \]  
(C.166)

Then, solve the above equation for \( \frac{\hat{v}_o(s)}{\hat{d}(s)} \) to yield
Apply the voltage divider technique to find the relation between \( \dot{d}(s) \) and \( \dot{v}_c(s) \),

\[
\dot{v}_c(s) = \frac{\left( \frac{D_1}{1-D+D_1} \right) V_c * Z_{eq}}{Z_{eq} + \left( \frac{D_1}{1-D+D_1} \right)^2 sL_1}
\]

(C.156)

Solving for \( \frac{\dot{v}_c(s)}{\dot{d}(s)} \) yields

\[
\frac{\dot{v}_c(s)}{\dot{d}(s)} = \frac{D_1 \left( 1-D+D_1 \right)V_c}{(1-D+D_1)^2 \left( s^2 L_o C_o + \frac{L_o}{R_L} + 1 \right) + s^4 L_i L_o C_i C_o + s^3 \frac{L_i L_o C_i}{R_L} + s^2 \left( D_1^2 L_i C_o + L_i C_1 \right) + s \frac{D_1^2 L_1}{R_L}}
\]

(C.157)

Finally, normalize the above equation to yield

\[
G_o(s) = \frac{\dot{v}_c(s)}{\dot{d}(s)}_{s(\dot{d})} = \frac{D_1 \left( 1-D+D_1 \right)V_c}{s^4 L_i L_o C_i C_o + s^3 \left( \frac{D_1^2 L_i C_o + L_i C_1}{R_L (1-D+D_1)} \right) + s^2 \left( \frac{D_1^2 L_i C_o + L_i C_1}{R_L (1-D+D_1)} \right) + s \left( \frac{D_1^2 L_1}{R_L (1-D+D_1)} \right) + 1}
\]

(C.158)

C.24 Control-to-Output Transfer Function (\( \dot{d}(t) \)-dependent voltage source deactivated)

The voltage divider technique is applied to find the relation between \( \dot{v}_o(s) \) and \( \dot{v}_c(s) \),

\[
\dot{v}_o(s) = \dot{v}_c(s) \frac{\left( \frac{R_L}{sC_o} \right)}{sL_o + \left( \frac{R_L}{sC_o} \right)}
\]

(C.160)

Normalizing the above equation, and solving for \( \dot{v}_o(s) \),
\[ T_{pi} = 2\pi \sqrt{L_1 C_1} >> D' T_S \]  \hspace{1cm} (C.173)

Then, \[ T_S << \frac{2\pi \sqrt{L_1 C_1}}{D'} \]  \hspace{1cm} (C.174)

Solving for \( L_1 \),

\[ L_1 = L_2 >> \frac{1}{C_1} \left( \frac{D'T_S}{2\pi} \right)^2 \]  \hspace{1cm} (C.175)

### C.26 Inductors Design (Upper Limit)

Upper limits of \( L_1 \) and \( L_2 \) depend on the reactances of \( L_1 \) and \( L_2 \), which must be less than the converter effective input resistance \( R_{i-eff} \),

\[ X_{L_1} << R_{i-eff} \]  \hspace{1cm} (C.176)

\[ 2\pi f_L L_1 << \frac{D^2 T_S}{2 C_1} \left( \frac{V_i}{V_i - V_o} \right) \]  \hspace{1cm} (C.177)

\[ L_1 << \frac{D^2 T_S}{4\pi f_L C_1} \left( \frac{V_i}{V_i - V_o} \right) \]  \hspace{1cm} (C.178)

Assuming \( V_o << V_i \),

\[ L_1 << \frac{R_{i-eff \omega L_1}}{\omega L_1} = \frac{D^2 T_S}{4\pi f_L C_1} \]  \hspace{1cm} (C.179)

### C.27 Equivalent Inductor Design

To maintain a constant output current during one switching cycle, the resonance time contact of the input capacitor \( C_1 \) and the equivalent inductors \( L_e \) must be much higher than the switch-on time.

From Fig. 3.10, the switch-off time is expressed by,

\[ T_{r_2} = t_{on} = D T_S \]  \hspace{1cm} (C.180)

At resonance time,
\[ \dot{v}_c(s) = \frac{D_1 I_1}{(1 - D + D_1)^2 \left( s^2 L_o C_o + s \frac{L_o}{R_L} + 1 \right) + s^4 L_1 L_o C_1 C_o + s^3 \frac{L_1 L_o C_1}{R_L} + s^2 \left( D_1^2 L_1 C_o + L_1 C_1 \right) + s \frac{D_1^2 L_1}{R_L}} \]

(C.167)

\[ \frac{\dot{v}_c(s)}{d(s)} = \frac{D_1 I_1}{s^4 L_1 L_o C_1 C_o + s^3 \frac{L_1 L_o C_1}{R_L} + s^2 \left( D_1^2 L_1 C_o + L_1 C_1 \right) + s \left( \frac{D_1^2 L_1}{R_L} + L_o \right) (1 - D + D_1)^2 + (0 - D + D_1)^2} \]

(C.168)

 Normalize the above equation to yield

\[ G_{ud}(s) = \frac{\dot{v}_c(s)}{d(s)} \bigg|_{(1 - D + D_1)^2} = \frac{D_1 I_1}{s^4 L_1 L_o C_1 C_o + s^3 \frac{L_1 L_o C_1}{R_L} + s^2 \left( D_1^2 L_1 C_o + L_1 C_1 \right) + s \left( \frac{D_1^2 L_1}{R_L} + L_o \right) + 1} \]

(C.169)

The control-to-output \( G_{ud}(s) \) transfer function is the summation of eqs. (3.92) and (3.94),

\[ G_{ud}(s) = \frac{\dot{v}_c(s)}{d(s)} \bigg|_{(1 - D + D_1)^2} = \frac{D_1 I_1}{s^4 L_1 L_o C_1 C_o + s^3 \frac{L_1 L_o C_1}{R_L} + s^2 \left( D_1^2 L_1 C_o + L_1 C_1 \right) + s \left( \frac{D_1^2 L_1}{R_L} + L_o \right) + 1} \]

(C.170)

**C.25 Inductors Design (Lower Limit)**

Lower limits of \( L_1 \) and \( L_2 \); To avoid resonance with the input capacitors \( C_1 \) and \( C_2 \) during switch-off time, the time constant of \( L_1 \) and \( C_1 \) must be greater than the switching-off time.

From Fig. 3.10, the switch-off time is expressed by,

\[ T_{r1} = t_{off} = (1 - D)T_s = D'T_s \]

(C.171)

While at resonance time,

\[ X_{C_1} = X_{L1} \]

(C.172)
\[ C_O = \frac{1}{\Delta v_o} \left( \frac{\eta V_o}{R_{l_{\text{eff}}} M^2} \left( \frac{t}{2} - \frac{\sin(2 \omega_L t)}{4 \omega_L} - \frac{\sin(2 \omega_L t)}{4 \omega_L} \right) \right)^{3T_e/8} \]  \hspace{1cm} (C.191)

\[ C_O = \frac{V_o}{\Delta v_o} \left( \frac{\eta}{R_{l_{\text{eff}}} M^2} \left( \frac{3T_e}{8} - \frac{\sin\left(\frac{3\pi}{4}\right)}{4\omega_L} - \frac{T_e}{16} + \frac{\sin\left(\frac{\pi}{4}\right)}{4\omega_L} \right) - \frac{3T_e}{8R_L} + \frac{T_L}{8R_L} \right) \]  \hspace{1cm} (C.192)

\[ C_O = \frac{T_L V_o}{4 \Delta v_o} \left[ \frac{\eta}{R_{l_{\text{eff}}} M^2} \left( \frac{1}{\pi} + 1 \right) - \frac{1}{R_L} \right] \]  \hspace{1cm} (C.193)
Then, \( T_S \ll \frac{2\pi \sqrt{L_c C_1}}{D} \)

Solving for \( L_c \),

\[
L_c \gg \frac{1}{C_1} \left( \frac{DT_S}{2\pi} \right)^2
\]

### C.28 Output Inductor Current

To find the output current \( i_{Lo}(t) \) as a function of time,

\[
P_o = \eta P_m
\]

\[
V_o i_{Lo}(t) = \eta \frac{V_m^2(t)}{R_{l_{-eff}}}
\]

\[
i_{Lo}(t) = \frac{\eta V_o^2}{V_o R_{l_{-eff}}} \sin^2(\omega t)
\]

Multiplying by \( \frac{V_o}{V_o} \), and substituting by eq. (3.42),

\[
i_{Lo}(t) = \frac{\eta V_o}{M^2 R_{l_{-eff}}} \sin^2(\omega t)
\]

### C.29 Output Capacitor Design

The output capacitor \( C_o \) value, which is required to maintain a peak-peak output voltage ripple of 0.6\% of \( V_o \), and referring to eq. (4.9), is given by,

\[
C_o = \frac{1}{\Delta V_o} \int_{T_L/8}^{3T_L/8} \frac{\eta V_o}{R_{l_{-eff}}} M^2 \sin^2(\omega_L t) - \frac{V_o}{R_L} dt \quad (C.189)
\]

\[
C_o = \frac{1}{\Delta V_o} \int_{T_L/8}^{3T_L/8} \left( \frac{\eta V_o}{M^2 R_{l_{-eff}}} \sin^2(\omega_L t) - \frac{V_o}{R_L} \right) dt \quad (C.190)
\]


REFERENCES


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محول باك الالمنقَطّر ذو معامل القدرة العالي الذي يعمل خلال وضع جهد المكثف المتقطع

الخلاصة

إن مصادر الطاقة التي تدعم تقنيات تحسين معامل القدرة أصبحت حاجة ملحة في كثير من الأجهزة الإلكترونية لتلبية اللوائح والمعايير التوافقية مثل اللجنة الكهربائية التكنولوجية الدولية أي سي 61000-3.

وفي محاولة لتحقيق أقصى قدر من الكفاءة لمصادر الطاقة، تم توجيه الجهود البحثية لتصميم دوائر مصادر الطاقة الالمنقَطّرة والتي تدعم معامل القدرة حيث تم تقليل عدد مكونات الدوائر من أشباه الموصلات والتي تولد خسائر وذل ذلك بتحليل عدد الدوارات أو الاصطدامات الثنائية في دوائر المغناطيسية الكامنة. تسمح دوائر الطاقة الالمنقَطّرة بتدفق تيار كهربائي من خلال حد أدنى من المفاتيح الإلكترونية بالمقارنة مع دوائر تحسين معامل القدرة التقليدية. وفقا لذلك، يمكن تخفيف خسائر التوصيل بشكل ملحوظ ويمكن الحصول على كفاءة عالية، فضلا عن وفرات في التكاليف.

لقد تم تقديم تصاميم عدة لدوائر مصادر طاقة لمنقَطعات داعمة لتكون معامل القدرة، وتتحسن كفاءة القدرة كمعدلة و/أو خفض ابعادات الضوضاء عبر تقنيات مفاتيح سلسة أو طبولوجيا مغناطيسية مقترنة. إلا أن كل هذه التصاميم تعمل في وضع دي أي سي إم أو وضع تيار المحت منقَطع. إن وضع تيار المحت منقَطع له شعبيات عالية نظرًا لتناسق خصائص تحسين معامل القدرة التشغيل السلس وتحكم غير معقد. إلا أن وضع تيار المحت منقَطع يعني من تقطيع تيار الدخول وإجهادات عالية لتيارات المفاتيح.

من جهة أخرى، فإن دوائر وضع جهد المكثف المتقطع تمتع بكثير من المزايا الجاذبة وتقدم فوائد عدة. فلها مقترح على إغلاق المفاتيح بشكل سلس وبالتالي فإن ترانزستور توغ أي جي بي يفي بالغرض كمفتاح تشغيلي. كما أنها تمتلك ميزة تيار الدخول الغير منقَطع و بالتالي لا يوجد حاجة لإستعمال مرشحات الدخول. لقد تم عمل الكثير من الدراسات على دوائر وضع جهد المكثف المتقطع غير أن كلها تحتوي نظرة كاملة في دائرة المصدر.

في هذه الدراسة، سنعرض محول باك جديد لمنقَطع يعمل خلال وضع جهد المكثف المتقطع. الدائرة الجديدة لها نفس الميزات لجميع دوائر جهد المكثف المتقطع، إلا أن استخدام مقوم لمنقَطع في بداية الدائرة يقلل من خسائر التوصيل وبالتالي يحسن الكفاءة بشكل ملحوظ.

بقول: نصر الله "محمد عوني" خريم

كانون ثاني 2013
جامعة الإمارات العربية المتحدة
كلية الهندسة
برنامج ماجستير الهندسة الكهربائية

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إعداد:
نصر الله "محمد عوني" خريم

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مشرف الرسالة:
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